# Novena PVT2-A

## Power sequencing

| rail name | voltage | dependent blocks | sheet | derived from | sequence | generated by | capacity | notes |
|---|---|---|---|---|---|---|---|---|
| RAW_PWR | 7V-17V | 5V master | 05pwr_input | external | 0 | AC adapter | 3A | when using only AC adapter, 12V nominal |
| BATT_PWR | 6V-18V | 5V master | 05pwr_input | external<br>external | 0<br>0 | AC adapter<br>battery pack | 3A – 6A | 3- and 4- cell Li-Ion are preferred configurations |
| P5.0V | 5V | 3.3V master<br>VTT regulator | 05pwr_input | BATT_PWR | 1 | NCP3020B | 7A | |
| P5.0V_DELAYED | 5V | SATA connector<br>USB ports<br>USB hub (master & slave) *<br>USB_OTG_VBUS<br>HDMI 5V<br>Speaker amplifiers<br>PWM I/O block (option)<br>ADC 3.3V regulator<br>expansion header | 05pwr_input | P5.0V | 6 | SI4435DY | 7A | delay control is P2.5V_VGEN5<br><br>to power unused 3.3V regulator circuit |
| P3.3V | 3.3V | DDR3 SO-DIMM<br>PMIC VIN3<br>PMIC SW inputs<br>Battery interface voltages<br>MCU Reset | 05pwr_input | P5.0V | 1 | FAN53540UCX | 5A | |
| P3.3V_DELAYED | 3.3V | NVCC_LCD<br>NVCC_GPIO<br>NVCC_SD1, 2 and 3<br>NVCC_NANDF<br>NVCC_JTAG<br>NVCC_EIM0, 1, and 2<br>PMIC_VIN2<br>Boot config straps<br>JTAG<br>internal MicroSD pawitch<br>external SD card<br>utility EEPROM<br>USB hub (master & slave)<br>SATA connector<br>100Mbit ethernet<br>PCIE pawitch<br>LCD panel<br>digital microphone<br>audio codec pawitch<br>FPGA I/O<br>FPGA expansion I/O<br>Apoptosis circuit<br>FPGA serial memories<br>accelerometer<br>expansion header<br>UART 3,4 headers via schottky | 05pwr_input | P3.3V | 6 | SI4435DY | 5A | delay control is P2.8V_VGEN6<br><br>actual voltage closer to 2.8V-3.0V |

| rail name | voltage | dependent blocks | sheet | derived from | sequence | generated by | capacity | notes |
|---|---|---|---|---|---|---|---|---|
| VCC_1.2V_SW1AB | 1.35V | VDDARM_IN, VDDARM23_IN | 02cpu_power | P3.3V | 3 | PMIC | 2.5A | starts at 1.375V |
| VDD_SOC_IN_SW1C | 1.225V | VDDSOC_IN | 02cpu_power | P3.3V | 3 | PMIC | 1.75A | starts at 1.375V |
| P3.0V_VDDHIGH_SW2 | 3.0V | VDDHIGH_IN<br>VIN1 of PMIC | 02cpu_power | P3.3V | 4 | PMIC | 2A | virtually unused |
| P1.5V_DDR_SW3 | 1.5V | DDR3 on SoC<br>DDR3 SO-DIMM<br>VTT regulator reference | | | 5 | PMIC | 2.5A | |
| P1.8V_SW4 | 1.8V | | 04pwr_pmic | P3.3V | 5 | PMIC | 1A | unused! |
| P3.3V_STBY_RST | 5V | | 04pwr_pmic | P3.3V | soft | PMIC | 0.5A | unused! |
| P1.2V_VGEN1 | 1.2V | | 04pwr_pmic | P3.0V_VDDHIGH_SW2 | soft | PMIC | 0.1A | unused! |
| P1.5V_VGEN2 | 1.5V | PCI-express | 04pwr_pmic | P3.0V_VDDHIGH_SW2 | 4 | PMIC | 0.25A | note PCIE spec is 0.375A |
| P1.8V_VGEN3 | ?? | | 04pwr_pmic | P3.3V_DELAYED | soft | PMIC | 0.1A | 1.8V by BSP, not startup sequenced |
| P1.8V_VGEN4 | 1.8V | | 04pwr_pmic | P3.3V_DELAYED | 5 | PMIC | 0.35A | unused! |
| P2.5V_VGEN5 | 2.5V | Power-on LED<br>P5.0V_DELAYED control<br>RGMII I/O<br>NVCC_ENET<br>NVCC_RGMII<br>NVCC_CSI | 04pwr_pmic | P3.3V | 5 | PMIC | 0.1A | 1.5mA to LED<br><br>37 mA to PHY |
| P2.8V_VGEN6 | 2.8V | P3.3V_DELAYED control | 04pwr_pmic | P3.3V | 5 | PMIC | 0.2A | |
| P3.3V_LICELL | 2.5-3.3V | 0.08F supercap<br>P3.0V_STBY | 04pwr_pmic | P3.3V | 1 | PMIC | 0.00006A | ** override 2.5V default to 3.3V |
| P3.0V_STBY | 3.0V | CPU boot pins | 04pwr_pmic | P3.3V & P3.3V_LICELL | 2 | PMIC | 0.0004A | (VSNVS) |
| P0.75V_REFDDR | 0.75V | VTT regulator | 03cpu_sodimm | P1.5V_DDR_SW3 | 5 | PMIC | 0.015A | |
| P0.75V_DDR3_VTT | 0.75V | DDR3 SO-DIMM | 03cpu_sodimm | P5.0V | 6 | RT9046GSP | 1.5A | controlled by P0.75V_DDR3_VTT |
| SDCARD_VDD | 3.3V | microSD card | 07sdcard | P3.3V_DELAYED | soft | FDN304P | 0.2A | controlled by SD3_RST |
| EN1G_P1.2V | 1.2V | Gigabit ethernet | 11ethernet6bit | P5.0V | soft | LMR10510YSD | 1A | delay control is P3.3V_DELAYED |
| EN1G_P1.2VA | 1.2V | Gigabit ethernet | 11ethernet6bit | EN1G_P1.2V | soft | Ferrite bead | 1A | |
| EN1G_3.3VA | 3.3V | Gigabit ethernet | 11ethernet6bit | P3.3V_DELAYED | 5 | Ferrite bead | | |
| P5.0V_SATA | 5V | SATA connector | 09sata | P5.0V_DELAYED | soft | SI4435DY | 2A | SATA_PWRON manual control |
| EN100_A3.3V | 3.3V | 100Mbit ethernet | 10ethernet100 | P3.3V_DELAYED | 6 | Ferrite bead | 0.5A | |
| EN100_D1.8V | 1.8V | 100Mbit ethernet | 10ethernet100 | P3.3V_DELAYED | 6 | AX88772B | | |
| EN100_A1.8V | 1.8V | 100Mbit ethernet | 10ethernet100 | P3.3V_DELAYED | 5 | Ferrite bead | | |
| MPCIE_3.3V | 3.3V | PCI-express | 12mPCIe | P3.3V_DELAYED | soft | FDN304P | 1A | PCIE_PWRON manual control |
| UIM_PWR | 3.3V | UIM | 12mPCIe | P3.3V_DELAYED | soft | FDN304P | 0.1A | UIM_PWRON control; beware conflict with mPCIE sourcing |
| TX_HDMI_5V | 5V | HDMI | 13hdmi_lcd | P5.0V_DELAYED | 5 | 50mA fuse | 0.05A | |
| LCD_VCC_SW | 3.3V | LCD panel | 13hdmi_lcd | P3.3V_DELAYED | soft | SI4435DY | 2A | LCD_PWR_CTL; note active pulldown during power-off |
| LCD_BL_VDD | 6V-18V | LCD backlight | 13hdmi_lcd | BATT_PWR | soft | SI4435DY | 2A | LCD_PWR_CTL for master power cutoff |
| AUD_P3.3V | 3.3V | audio codec | 14audio | P3.3V_DELAYED | soft | FDN304P | 0.5A | AUD_PWRON; note active pulldown during power-off |
| P1.2V | 1.2V | FPGA core | 15fpga | P5.0V_DELAYED | 6 | LMR10510YSD | 1A | always on |
| VANA | 3.3V | ADC | 15fpga | P5.0V_DELAYED | 6 | LP2980IM5-3.3 | 0.05A | always on |

| rail name | voltage | dependent blocks | sheet | derived from | sequence | generated by | capacity | notes |
|---|---|---|---|---|---|---|---|---|
| P5.0V_WIFI | 5V | USB wifi option | 08usb | P5.0V_DELAYED | soft | RT9706 | 0.5A | USB_PWREN3_N off of main hub |
| P5.0V_USBEXT1 | 5V | external USB | 08usb | P5.0V_DELAYED | soft | RT9711BGB | 1.5A | USB_PWREN1_N off of main hub |
| P5.0V_USBEXT2 | 5V | external USB | 08usb | P5.0V_DELAYED | soft | RT9711BGB | 1.5A | USB_PWREN5_N off of slave hub |
| P5.0V_MOUSE | 5V | mouse | 08usb | P5.0V_DELAYED | soft | RT9706 | 0.5A | USB_PWREN7_N off of slave hub |
| P5.0V_KBD | 5V | keyboard | 08usb | P5.0V_DELAYED | soft | RT9706 | 0.5A | USB_PWREN8_N off of slave hub |
| USB_VID_P5V | 5V | video camera | 13hdmi_lcd | P5.0V_DELAYED | soft | RT9706 | 0.5A | USB_PWREN6_N off of slave hub |

P1.8V_SW4 has option to power VTT
Use this option to lower VTT source to 1.0V to save power

changes on table:

P1.8V_VGEN3 micbias gen option
(reprogram to 3.0V before using)

## I2C mappings:

addresses are already shifted left by one to accommodate r/w bit
i.e., address is expressed as the write address

I2C1: 10k pull-up
- SMBus functions (optional)
- MMA8452 (0x38) (optional)
- SO-DIMM identification (0xA0)
- FPGA (optional)
- SO-DIMM temp sensor (0x30) (optional)
- STMPE610 (0x88) (optional)
- Gas gauge and charger via SMB (on battery board)
- PCF8523 RTC (0xD0)

I2C2: 1.8k pull-up
- HDMI DDC (0xA0, 0x74)
- expansion header
- FPGA (optional)
- PMIC (0x10)

I2C3: 2.2k pull-up
- LCD EDID (0xA0)
- ES8283 (0x22)
- FPGA (optional)
- Utility EEPROM (0xAC)

U_02cpu_power — 02cpu_power.sch
U_03cpu_sodimm — 03cpu_sodimm.sch
U_04pwr_pmic — 04pwr_pmic.sch
U_05pwr_input — 05pwr_input.sch
U_06cpu_soc — 06cpu_soc.sch
U_07sdcard — 07sdcard.sch
U_08usb — 08usb.sch
U_09sata — 09sata.sch
U_10ethernet100 — 10ethernet100.sch
U_11ethernetGbit — 11ethernetGbit.sch
U_12mPCIe — 12mPCIe.sch
U_13hdmi_lcd — 13hdmi_lcd.sch
U_14audio — 14audio.sch
U_15fpga — 15fpga.sch
U_16gpio_misc — 16gpio_misc.sch



Sheet: /
File: 01docmap.sch

Title: 01docmap — Novena PVT2-A

| Size: B | Date: 22 12 2014 | Rev: |
|---|---|---|
| KiCad E.D.A. eeschema (2014-08-05 BZR 5054)-product | | Id: 1/16 |

Note: 22uF, 6.3V 0603 cap is TDK C1608X5R0J226M

U100
iMX6Q – MCIMX6Q5EYM12AC

i.MX6Q – POWER

1.375V (power-on), 1.35V (nominal)
SW1A/B

no support for i.MX6D – launch SKUs are Q and DL
i.MX6 Q DL S: short
i.MX6 D: open

i.MX6 Q DL S: open
i.MX6 D: short

1.375V (power-on), 1.225V (nominal)
SW1C

SW2

3.0V

D10C
RB751V40,115

VDD_SNVS_IN

C71C 0.22uF, 6.3V, X5R 10%

VDDARM_IN_1
VDDARM_IN_2
VDDARM_IN_3
VDDARM_IN_4
VDDARM_IN_5
VDDARM_IN_6
VDDARM_IN_7
VDDARM_IN_8

VDDARM23_IN_1
VDDARM23_IN_2
VDDARM23_IN_3
VDDARM23_IN_4
VDDARM23_IN_5
VDDARM23_IN_6
VDDARM23_IN_7
VDDARM23_IN_8

VDDSOC_IN_1
VDDSOC_IN_2
VDDSOC_IN_3
VDDSOC_IN_4
VDDSOC_IN_5
VDDSOC_IN_6
VDDSOC_IN_7
VDDSOC_IN_8
VDDSOC_IN_9
VDDSOC_IN_10

VDDHIGH_IN_1
VDDHIGH_IN_2

GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79

VDDARM_CAP_1 VDDARM_CAP_2 VDDARM_CAP_3 VDDARM_CAP_4 VDDARM_CAP_5 VDDARM_CAP_6 VDDARM_CAP_7 VDDARM_CAP_8
VDDARM_CAP23_1 VDDARM_CAP23_2 VDDARM_CAP23_3 VDDARM_CAP23_4 VDDARM_CAP23_5 VDDARM_CAP23_6 VDDARM_CAP23_7 VDDARM_CAP23_8
VDDSOC_CAP_1 VDDSOC_CAP_2 VDDSOC_CAP_3 VDDSOC_CAP_4 VDDSOC_CAP_5 VDDSOC_CAP_6 VDDSOC_CAP_7
VDDPU_CAP_1 VDDPU_CAP_2 VDDPU_CAP_3 VDDPU_CAP_4 VDDPU_CAP_5 VDDPU_CAP_6 VDDPU_CAP_7
VDD_CACHE_CAP
VDDHIGH_CAP_1 VDDHIGH_CAP_2
VDD_SNVS_CAP
NVCC_LCD
NVCC_CSI
NVCC_MIPI
NVCC_EIM0
NVCC_EIM1
NVCC_EIM2
NVCC_ENET
NVCC_GPIO
NVCC_PLL_OUT
NVCC_RGMII
NVCC_SD1
NVCC_SD2
NVCC_SD3
NVCC_NANDF
NVCC_JTAG
GPANAIO
FA_ANA
VDD_FA

VDD_ARM_CAP -1.2V
supplied by internal regulator
i.MX6 Q DL S: short
i.MX6 D: open
i.MX6 Q DL S: open
i.MX6 D: short
-1.2V
supplied by internal regulator
-1.2V
supplied by internal regulator
-2.5V
supplied by internal regulator
supplied by internal regulatorVDD_SNVS_CAP
NVCC_PLL_OUT

J10C
J11C
J12C
test point (DNP)

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Kosagi Novena PVT2-A
Sheet: /U_02cpu_power/
File: 02cpu_power.sch
Title: 02cpu_power
Size: C | Date: 22 12 2014 | Rev:
KiCad E.D.A. eeschema (2014-08-05 BZR 5054)-product | Id: 2/16

U100_2
iMX6Q – MCIMX6Q5EYM12AC

i.MX6Q – DDR

| | | | | | |
|---|---|---|---|---|---|
| DDR_D0 | DDR3_D0 | AD2 | DRAM_D0 | DRAM_A0 | AC14 DDR3_A0 DDR_CTL |
| DDR_D0 | DDR3_D1 | AE2 | DRAM_D1 | DRAM_A1 | AB14 DDR3_A1 DDR_CTL |
| DDR_D0 | DDR3_D2 | AC4 | DRAM_D2 | DRAM_A2 | AA14 DDR3_A2 DDR_CTL |
| DDR_D0 | DDR3_D6 | AA5 | DRAM_D3 | DRAM_A3 | Y14 DDR3_A3 DDR_CTL |
| DDR_D0 | DDR3_D4 | AC1 | DRAM_D4 | DRAM_A4 | W14 DDR3_A4 DDR_CTL |
| DDR_D0 | DDR3_D5 | AD1 | DRAM_D5 | DRAM_A5 | AE13 DDR3_A5 DDR_CTL |
| DDR_D0 | DDR3_D3 | AB4 | DRAM_D6 | DRAM_A6 | AC13 DDR3_A6 DDR_CTL |
| DDR_D0 | DDR3_D7 | AE4 | DRAM_D7 | DRAM_A7 | Y13 DDR3_A7 DDR_CTL |
| | DDR3_DQS0_P | AE3 | DRAM_SDQS0 | DRAM_A8 | AB13 DDR3_A8 DDR_CTL |
| | DDR3_DQS0_N | AD3 | DRAM_SDQS0_B | DRAM_A9 | AE12 DDR3_A9 DDR_CTL |
| DDR_D0 | DDR3_DM0 | AC3 | DRAM_DQM0 | DRAM_A10 | AA15 DDR3_A10 DDR_CTL |
| | | | | DRAM_A11 | AC12 DDR3_A11 DDR_CTL |
| DDR_D1 | DDR3_D8 | AD5 | DRAM_D8 | DRAM_A12 | AD12 DDR3_A12 DDR_CTL |
| DDR_D1 | DDR3_D12 | AE5 | DRAM_D9 | DRAM_A13 | AC17 DDR3_A13 DDR_CTL |
| DDR_D1 | DDR3_D13 | AA6 | DRAM_D10 | DRAM_A14 | AA12 DDR3_A14 DDR_CTL |
| DDR_D1 | DDR3_D14 | AE7 | DRAM_D11 | DRAM_A15 | Y12 DDR3_A15 DDR_CTL |
| DDR_D1 | DDR3_D11 | AB5 | DRAM_D12 | | |
| DDR_D1 | DDR3_D15 | AC5 | DRAM_D13 | DRAM_SDBA0 | AC15 DDR3_BA0 DDR_CTL |
| DDR_D1 | DDR3_D9 | AB6 | DRAM_D14 | DRAM_SDBA1 | Y15 DDR3_BA1 DDR_CTL |
| DDR_D1 | DDR3_D10 | AC7 | DRAM_D15 | DRAM_SDBA2 | AB12 DDR3_BA2 DDR_CTL |
| | DDR3_DQS1_P | AD6 | DRAM_SDQS1 | | |
| | DDR3_DQS1_N | AE6 | DRAM_SDQS1_B | | |
| DDR_D1 | DDR3_DM1 | AC6 | DRAM_DQM1 | | |
| DDR_D2 | DDR3_D16 | AB7 | DRAM_D16 | DRAM_CS0 | Y16 DDR3_CS0 DDR_CTL |
| DDR_D2 | DDR3_D22 | AA8 | DRAM_D17 | DRAM_CS1 | AD17 DDR3_CS1 DDR_CTL |
| DDR_D2 | DDR3_D19 | AB9 | DRAM_D18 | | |
| DDR_D2 | DDR3_D21 | Y9 | DRAM_D19 | | |
| DDR_D2 | DDR3_D18 | Y7 | DRAM_D20 | DRAM_RAS | AB15 DDR3_RAS DDR_CTL |
| DDR_D2 | DDR3_D23 | Y8 | DRAM_D21 | DRAM_CAS | AE16 DDR3_CAS DDR_CTL |
| DDR_D2 | DDR3_D17 | AC8 | DRAM_D22 | DRAM_SDWE | AB16 DDR3_WE DDR_CTL |
| DDR_D2 | DDR3_D20 | AA9 | DRAM_D23 | | |
| | DDR3_DQS2_P | AD8 | DRAM_SDQS2 | | |
| | DDR3_DQS2_N | AE8 | DRAM_SDQS2_B | DRAM_SDCKE0 | Y11 DDR3_CKE0 DDR_CTL |
| DDR_D2 | DDR3_DM2 | AB8 | DRAM_DQM2 | DRAM_SDCKE1 | AA11 DDR3_CKE1 DDR_CTL |
| DDR_D3 | DDR3_D24 | AE9 | DRAM_D24 | DRAM_SDODT0 | AC16 DDR3_ODT0 DDR_CTL |
| DDR_D3 | DDR3_D27 | Y10 | DRAM_D25 | DRAM_SDODT1 | AB17 DDR3_ODT1 DDR_CTL |
| DDR_D3 | DDR3_D25 | AE11 | DRAM_D26 | | |
| DDR_D3 | DDR3_D26 | AB11 | DRAM_D27 | | |
| DDR_D3 | DDR3_D31 | AC9 | DRAM_D28 | | |
| DDR_D3 | DDR3_D29 | AD9 | DRAM_D29 | | |
| DDR_D3 | DDR3_D28 | AD11 | DRAM_D30 | DRAM_RESET | Y6 DDR3_RESET DDR_CTL |
| DDR_D3 | DDR3_D30 | AC11 | DRAM_D31 | | |
| | DDR3_DQS3_P | AC10 | DRAM_SDQS3 | | |
| | DDR3_DQS3_N | AB10 | DRAM_SDQS3_B | | |
| DDR_D3 | DDR3_DM3 | AE10 | DRAM_DQM3 | | |
| DDR_D4 | DDR3_D32 | AA17 | DRAM_D32 | DRAM_SDCLK_0 | AD15 DDR3_CK0_P DIFFPAIR DDR_CLK0 |
| DDR_D4 | DDR3_D38 | AA18 | DRAM_D33 | DRAM_SDCLK_0_B | AE15 DDR3_CK0_N DIFFPAIR |
| DDR_D4 | DDR3_D39 | AC18 | DRAM_D34 | | |
| DDR_D4 | DDR3_D33 | AE19 | DRAM_D35 | | |
| DDR_D4 | DDR3_D36 | Y17 | DRAM_D36 | | |
| DDR_D4 | DDR3_D34 | Y18 | DRAM_D37 | | |
| DDR_D4 | DDR3_D37 | AB19 | DRAM_D38 | | |
| DDR_D4 | DDR3_D35 | AC19 | DRAM_D39 | | |
| | DDR3_DQS4_P | AD18 | DRAM_SDQS4 | | |
| | DDR3_DQS4_N | AE18 | DRAM_SDQS4_B | DRAM_SDCLK_1 | AD14 DDR3_CK1_P DIFFPAIR DDR_CLK1 |
| DDR_D4 | DDR3_DM4 | AB18 | DRAM_DQM4 | DRAM_SDCLK_1_B | AE14 DDR3_CK1_N DIFFPAIR |
| DDR_D5 | DDR3_D40 | Y19 | DRAM_D40 | | |
| DDR_D5 | DDR3_D41 | AB20 | DRAM_D41 | | |
| DDR_D5 | DDR3_D42 | AB21 | DRAM_D42 | | |
| DDR_D5 | DDR3_D44 | AD21 | DRAM_D43 | | |
| DDR_D5 | DDR3_D45 | Y20 | DRAM_D44 | | |
| DDR_D5 | DDR3_D43 | AA20 | DRAM_D45 | | |
| DDR_D5 | DDR3_D47 | AE21 | DRAM_D46 | | |
| DDR_D5 | DDR3_D46 | AC21 | DRAM_D47 | | |
| | DDR3_DQS5_P | AD20 | DRAM_SDQS5 | | |
| | DDR3_DQS5_N | AE20 | DRAM_SDQS5_B | | |
| DDR_D5 | DDR3_DM5 | AC20 | DRAM_DQM5 | | |
| DDR_D6 | DDR3_D48 | AC22 | DRAM_D48 | DRAM_VREF | AC2 |
| DDR_D6 | DDR3_D54 | AE22 | DRAM_D49 | | |
| DDR_D6 | DDR3_D50 | AE24 | DRAM_D50 | | |
| DDR_D6 | DDR3_D52 | AC24 | DRAM_D51 | | |
| DDR_D6 | DDR3_D53 | AB22 | DRAM_D52 | | |
| DDR_D6 | DDR3_D51 | AC23 | DRAM_D53 | ZQPAD | AE17 DDR3_ZQPAD |
| DDR_D6 | DDR3_D49 | AD25 | DRAM_D54 | | |
| DDR_D6 | DDR3_D55 | AC25 | DRAM_D55 | | |
| | DDR3_DQS6_P | AD23 | DRAM_SDQS6 | NVCC_DRAM_1 | R18 |
| | DDR3_DQS6_N | AE23 | DRAM_SDQS6_B | NVCC_DRAM_2 | T18 |
| DDR_D6 | DDR3_DM6 | AD24 | DRAM_DQM6 | NVCC_DRAM_3 | U18 |
| | | | | NVCC_DRAM_4 | V10 |
| DDR_D7 | DDR3_D56 | AB25 | DRAM_D56 | NVCC_DRAM_5 | V11 |
| DDR_D7 | DDR3_D57 | AA21 | DRAM_D57 | NVCC_DRAM_6 | V12 |
| DDR_D7 | DDR3_D58 | Y25 | DRAM_D58 | NVCC_DRAM_7 | V13 |
| DDR_D7 | DDR3_D61 | Y22 | DRAM_D59 | NVCC_DRAM_8 | V14 |
| DDR_D7 | DDR3_D60 | AB23 | DRAM_D60 | NVCC_DRAM_9 | V15 |
| DDR_D7 | DDR3_D59 | AA23 | DRAM_D61 | NVCC_DRAM_10 | V16 |
| DDR_D7 | DDR3_D63 | Y23 | DRAM_D62 | NVCC_DRAM_11 | V17 |
| DDR_D7 | DDR3_D62 | W25 | DRAM_D63 | NVCC_DRAM_12 | V18 |
| | DDR3_DQS7_P | AA25 | DRAM_SDQS7 | NVCC_DRAM_13 | V9 |
| | DDR3_DQS7_N | AA24 | DRAM_SDQS7_B | | |
| DDR_D7 | DDR3_DM7 | Y21 | DRAM_DQM7 | | |

C11M 0.01uF, 10V, X5R, 10%
C10M 0.22uF, 6.3V, X5R, 10%
+GND

C12M 2.2pF, NPO (DNP)
C13M 2.2pF, NPO (DNP)

R10M 10k, 1%

C16M 0.1uF, 6.3V, X5R

R11M 240, 1%

JP10M

| | | | | | |
|---|---|---|---|---|---|
| 1 | VREFDQ | VSS | 2 | | |
| 3 | VSS | DQ4 | 4 | DDR3_D4 | |
| DDR3_D0 | 5 | DQ0 | DQ5 | 6 | DDR3_D5 |
| DDR3_D1 | 7 | DQ1 | VSS | 8 | |
| | 9 | VSS | DQS0_N | 10 | DDR3_DQS0_NDIFFPAIR |
| DDR3_DM0 | 11 | DM0 | DQS0_P | 12 | DDR3_DQS0_PDIFFPAIR |
| | 13 | VSS | VSS | 14 | |
| DDR3_D2 | 15 | DQ2 | DQ6 | 16 | DDR3_D6 |
| DDR3_D3 | 17 | DQ3 | DQ7 | 18 | DDR3_D7 |
| | 19 | VSS | VSS | 20 | |
| DDR3_D8 | 21 | DQ8 | DQ12 | 22 | DDR3_D12 |
| DDR3_D9 | 23 | DQ9 | DQ13 | 24 | DDR3_D13 |
| | 25 | VSS | VSS | 26 | |
| DIFFPAIRDDR3_DQS1_N | 27 | DQS1_N | DM1 | 28 | DDR3_DM1 |
| DIFFPAIRDDR3_DQS1_P | 29 | DQS1_P | RESET_N | 30 | DDR3_RESET |
| | 31 | VSS | VSS | 32 | |
| DDR3_D10 | 33 | DQ10 | DQ14 | 34 | DDR3_D14 |
| DDR3_D11 | 35 | DQ11 | DQ15 | 36 | DDR3_D15 |
| | 37 | VSS | VSS | 38 | |
| DDR3_D16 | 39 | DQ16 | DQ20 | 40 | DDR3_D20 |
| DDR3_D17 | 41 | DQ17 | DQ21 | 42 | DDR3_D21 |
| | 43 | VSS | VSS | 44 | |
| DIFFPAIRDDR3_DQS2_N | 45 | DQS2_N | DM2 | 46 | DDR3_DM2 |
| DIFFPAIRDDR3_DQS2_P | 47 | DQS2_P | VSS | 48 | |
| | 49 | VSS | DQ22 | 50 | DDR3_D22 |
| DDR3_D18 | 51 | DQ18 | DQ23 | 52 | DDR3_D23 |
| DDR3_D19 | 53 | DQ19 | VSS | 54 | |
| | 55 | VSS | DQ28 | 56 | DDR3_D28 |
| DDR3_D24 | 57 | DQ24 | DQ29 | 58 | DDR3_D29 |
| DDR3_D25 | 59 | DQ25 | VSS | 60 | |
| | 61 | VSS | DQS3_N | 62 | DDR3_DQS3_NDIFFPAIR |
| DDR3_DM3 | 63 | DM3 | DQS3_P | 64 | DDR3_DQS3_PDIFFPAIR |
| | 65 | VSS | VSS | 66 | |
| DDR3_D26 | 67 | DQ26 | DQ30 | 68 | DDR3_D30 |
| DDR3_D27 | 69 | DQ27 | DQ31 | 70 | DDR3_D31 |
| | 71 | VSS | VSS | 72 | |
| DDR3_CKE0 | 73 | CKE0 | CKE1 | 74 | DDR3_CKE1 |
| | 75 | VDD | VDD | 76 | |
| | | | A15 | 78 | DDR3_A15 |
| DDR3_BA2 | 79 | BA2 | A14 | 80 | DDR3_A14 |
| | 81 | VDD | VDD | 82 | |
| DDR3_A12 | 83 | A12 | A11 | 84 | DDR3_A11 |
| DDR3_A9 | 85 | A9 | A7 | 86 | DDR3_A7 |
| | 87 | VDD | VDD | 88 | |
| DDR3_A8 | 89 | A8 | A6 | 90 | DDR3_A6 |
| DDR3_A5 | 91 | A5 | A4 | 92 | DDR3_A4 |
| | 93 | VDD | VDD | 94 | |
| DDR3_A3 | 95 | A3 | A2 | 96 | DDR3_A2 |
| DDR3_A1 | 97 | A1 | A0 | 98 | DDR3_A0 |
| | 99 | VDD | VDD | 100 | |
| DDR3_CK0_P | 101 | CK0_P | CK1_P | 102 | DDR3_CK1_P |
| DDR3_CK0_N | 103 | CK0_N | CK1_N | 104 | DDR3_CK1_N |
| | 105 | VDD | VDD | 106 | |
| DDR3_A10 | 107 | A10 | BA1 | 108 | DDR3_BA1 |
| DDR3_BA0 | 109 | BA0 | RAS_N | 110 | DDR3_RAS |
| | 111 | VDD | VDD | 112 | |
| DDR3_WE | 113 | WE_N | S0_N | 114 | DDR3_CS0 |
| DDR3_CAS | 115 | CAS_N | ODT0 | 116 | DDR3_ODT0 |
| | 117 | VDD | VDD | 118 | |
| DDR3_A13 | 119 | A13 | ODT1 | 120 | DDR3_ODT1 |
| DDR3_CS1 | 121 | S1_N | | | |
| | 123 | VDD | VDD | 124 | |
| | 125 | | VREFCA | 126 | |
| | 127 | VSS | VSS | 128 | |
| DDR3_D32 | 129 | DQ32 | DQ36 | 130 | DDR3_D36 |
| DDR3_D33 | 131 | DQ33 | DQ37 | 132 | DDR3_D37 |
| | 133 | VSS | VSS | 134 | |
| DIFFPAIRDDR3_DQS4_N | 135 | DQS4_N | DM4 | 136 | DDR3_DM4 |
| DIFFPAIRDDR3_DQS4_P | 137 | DQS4_P | VSS | 138 | |
| | 139 | VSS | DQ38 | 140 | DDR3_D38 |
| DDR3_D34 | 141 | DQ34 | DQ39 | 142 | DDR3_D39 |
| DDR3_D35 | 143 | DQ35 | VSS | 144 | |
| | 145 | VSS | DQ44 | 146 | DDR3_D44 |
| DDR3_D40 | 147 | DQ40 | DQ45 | 148 | DDR3_D45 |
| DDR3_D41 | 149 | DQ41 | VSS | 150 | |
| | 151 | VSS | DQS5_N | 152 | DDR3_DQS5_NDIFFPAIR |
| DDR3_DM5 | 153 | DM5 | DQS5_P | 154 | DDR3_DQS5_PDIFFPAIR |
| | 155 | VSS | VSS | 156 | |
| DDR3_D42 | 157 | DQ42 | DQ46 | 158 | DDR3_D46 |
| DDR3_D43 | 159 | DQ43 | DQ47 | 160 | DDR3_D47 |
| | 161 | VSS | VSS | 162 | |
| DDR3_D48 | 163 | DQ48 | DQ52 | 164 | DDR3_D52 |
| DDR3_D49 | 165 | DQ49 | DQ53 | 166 | DDR3_D53 |
| | 167 | VSS | VSS | 168 | |
| DIFFPAIRDDR3_DQS6_N | 169 | DQS6_N | DM6 | 170 | DDR3_DM6 |
| DIFFPAIRDDR3_DQS6_P | 171 | DQS6_P | VSS | 172 | |
| | 173 | VSS | DQ54 | 174 | DDR3_D54 |
| DDR3_D50 | 175 | DQ50 | DQ55 | 176 | DDR3_D55 |
| DDR3_D51 | 177 | DQ51 | VSS | 178 | |
| | 179 | VSS | DQ60 | 180 | DDR3_D60 |
| DDR3_D56 | 181 | DQ56 | DQ61 | 182 | DDR3_D61 |
| DDR3_D57 | 183 | DQ57 | VSS | 184 | |
| | 185 | VSS | DQS7_N | 186 | DDR3_DQS7_NDIFFPAIR |
| DDR3_DM7 | 187 | DM7 | DQS7_P | 188 | DDR3_DQS7_PDIFFPAIR |
| | 189 | VSS | VSS | 190 | |
| DDR3_D58 | 191 | DQ58 | DQ62 | 192 | DDR3_D62 |
| DDR3_D59 | 193 | DQ59 | DQ63 | 194 | DDR3_D63 |
| | 195 | VSS | VSS | 196 | |
| | 197 | SA0 | EVENT_N | 198 | DDR3_EVENT_N |
| | 199 | VDDSPD | SDA | 200 | SMB_SDA |
| | 201 | SA1 | SCL | 202 | SMB_SCL |
| | 203 | VTT | VTT | 204 | |

DDR3 SODIMM socket, reverse pinout

address 0xA0
C17M 0.22uF, 6.3V, X5R 10%

R12M 10k, 1%

C14M 0.01uF, 10V, X5R 10%
C15M 0.22uF, 6.3V, X5R 10%

C18M C19M C20M 0.22uF, 6.3V, X5R (CL31A476MQHNNNE)

C21M C22M C23M C24M C25M C26M C27M C28M C29M C30M C31M
0.22uF, 6.3V, X5R 10%
0.01uF, 10V, X5R 10%
22uF, 6.3V, X5R 20%

C32M C33M C34M C35M C36M C37M C38M C39M
0.22uF, 6.3V, X5R (CL31A476MQHNNNE)
0.01uF, 10V, X5R 10%

C40M 0.1uF, 6.3V, X5R

C41M C42M C43M C44M C45M C46M C47M C48M C49M C50M C51M C52M C53M
1.0uF, 25V, 20% X5R (CL31A476MQHNNNE)

C54M 1.0uF, 25V, 20% X5R

R13M 2.2 ohm, 5%

U10M
RT9045GSP
VIN GND REFEN VOUT GND VCNTL

R15M 0 ohm, 0805
R16M 0 ohm, 0805 (DNP)
R14M 1k, 1%
C55M C56M 10uF, 10V, X5R, 20%

VTT_VCNTL

Option: SW4 power supply instead of SW3 to reduce VTT power:
SW4 is unused, so reprogram in BSP to 1.1V
(Approx 0.3–0.4V min drop-out @ 0.5A, 100C))



Sheet: /U_03cpu_sodimm/
File: 03cpu_sodimm.sch

**Title: 03cpu_sodimm**

Size: B | Date: 22 12 2014 | Rev:
KiCad E.D.A. eeschema (2014-08-05 BZR 5054)-product | Id: 3/16

POR default = 1.5V

POR default = 1.8V
for low-voltage eMMC

POR default = 2.5V

POR default = 2.8V

U200
MMPF0100NPAEP
VIN1
VIN2
VIN3
VREFDDR
VINREFDDR
VHALF
VGEN1
VGEN2
VGEN3
VGEN4
VGEN5
VGEN6
LICELL
VSNVS

POR default = 3.0V

POR default = 1.375V

U200_2
MMPF0100NPAEP
SW1FB
SW1AIN
SW1ALX
SW1BLX
SW1BIN
SW1CLX
SW1CIN
SW1CFB
SW1VSSSNS
SW2LX
SW2IN_1
SW2IN_2
SW2FB
EPGND
GNDREF1
SW3AFB
SW3AIN
SW3ALX
SW3BLX
SW3BIN
SW3BFB
SW3VSSSSNS
SW4FB
SW4IN
SW4LX
SWBSTLX
SWBSTIN
SWBSTFB

POR default = 1.375V

POR default = 1.5V

POR default = 1.8V

POR default = 3.0V

+8V on J10P to program OTP
Remove R15P, populate R17P, C52P, C53P to progr
Remove R15P, R17P, populate R16P, C52P, C53P to boot from s
test point (DNP)

U10P
PCF8523T/1
OSCI
OSCO
VBAT
VSS
VDD
INT1/CLK
SCL
SDA

Must configure CL = 12.5pF via I2C!
Abracon ABS06-32.768KHZ-T 12.5pF CL

Device address = 0xD0/0xD1

U200_3
MMPF0100NPAEP
VIN
VCOREDIG
VCOREREF
VCORE
GNDREF
VDDOTP
VDDIO
SCL
SDA
PWRON
RESETBMCU
STANDBY
SDWNB
INTB
ICTEST

PMIC_PWRON
RESETBMCU
PMIC_STBY_REQ
PMIC_SDWNB
PMIC_INT_B
PMIC_ON_REQ
DDC_SCL
DDC_SDA
SMB_SCL
SMB_SDA

D10P
power LED
APT1608EC/red

BT10P
ML-621S/DN (DNP)

BT11P
BR1225A/FAN



| | |
|---|---|
| Sheet: /U_04pwr_pmic/ | |
| File: 04pwr_pmic.sch | |
| **Title: 04pwr_pmic** | |
| Size: B | Date: 22 12 2014 |
| KiCad E.D.A. eeschema (2014-08-05 BZR 5054)-product | Id: 4/16 |

Woven EVT2-A

Note: Do not use JP10N power plug when plugged into charger/battery board via J10N!!! Note: use R31N only in fixed installations. Remove if used with battery (rely on battery MCU to guarantee input cap discharge)

JP10N
2.1mm x 5.5mm DC jack
12V @ 3A
7V–19V nominal range
2.5A typ max 3A peak @ 12V
Absolute max rating is 25V

RAW_PWR
D11N PESD24VL1BA
C10N 0.1uF, 25V, X5R
D10N SSB44-E3/52T
BATT_PWR
R31N 2.2k, 1%

DC power + battery –> 5V regulator

6V–18V battery header
Compatible with:
2–cell Li–Ion
3–cell Li–Ion (preferred)
4–cell Li–Ion (preferred)
6–cell lead acid
6 to 12 cell NiMH

J10N MOLEX 87703–0001 male
+12V, +12V, +12V, GND, OPT, GND, +5V, +5V, +5V, GND, GND, GND, +3.3V, +3.3V, +3.3V, GND, B+, B–, GND, A–, A+, GND

M10N M2 mounting hole
M11N M2 mounting hole
M12N M2 mounting hole
M13N M2 mounting hole
M14N M2 mounting hole
M15N M2 mounting hole

R39N 330, 1% CHG_PWRSWITCH
R22N 330, 1% BATT_NRST
R21N 330, 1% SMB_SCL
R23N 330, 1% SMB_SDA
R26N 330, 1% UART4_TXD
R27N 330, 1% UART4_RXD

R28N 47k, 1%
R30N 47k, 1%
D13N ESD5Z3.3T1
D14N ESD5Z3.3T1
D17N ESD5Z3.3T1
D15N ESD5Z3.3T1
D16N ESD5Z3.3T1

U11N NCP3020B
VCC, COMP, FB, GND, BST, HSDR, VSW, LSDR
C11N 0.1uF, 25V, X5R
C12N 1.0uF, 25V, 20% X5R
C13N 0.1uF, 25V, X5R
REG5V_BST
REG5V_HSDR
REG5V_VSW
REG5V_LSDR
REG5V_COMP
C18N 330pF, X7R, 10%
C19N 8.2 pF, NPO
R14N 68k, 1%
R18N 0 ohm
R20N 0 ohm (DNP)
R17N 0 ohm
R19N 15k, 1%
D12N BAT54T1
R10N 8.06 ohm, 1%
R11N 10k, 1%
U10N NTMFS4841NT1G
U12N NTMFS4C35NT1G
set OC trip @ ~15A
C24N 470pF, X7R, 10%
REG5V_FBK

C14N, C15N, C16N, C17N 22uF, 25V, X5R, 10% (DNP)

L10NB place within MSS1260 pad
3.3uH, XAL7030–322MEC
L10N 3.3uH, MSS1260–332NLJ (DNP)
R12N 100, 1%
R13N 20 ohms, 1%
R15N 63.4k, 1%
R16N 44.99k, 1%
C25N 330pF, X7R, 10%
R25N 8.66k, 1%
C26N DNP
C20N, C21N, C22N, C23N 22uF, 10V, X5R, 20%
5V @ 7A max

Q10N Si4435DY
R24N 100k, 1%
C27N 1.0uF, 25V, 20% X5R
R29N 10k, 1%
Q11N 2N7002W

5V –> 3.3V regulator

U13N FAN53541UCX
PGOOD, EN, MODE, VIN, VIN, VIN, VIN, FB, VOUT, SW, SW, SW, SW, AGND, GND
allow PFM
R34N 1k, 1%
R33N 1k, 1% (DNP)
R32N 1k, 1%
RESETBMCU
C31N 22uF, 10V, X5R, 20%
C32N 10nF, X7R, 50V, 10%
L11N 0.60uH, XAL4020–601ME
3.3V @ 5A max
C28N 22uF, 10V, X5R, 20%
C29N 10uF, 10V, X5R, 20% (DNP)
R36N 100k, 1%
3.33V nom
R37N 51.6k, 1%
R35N 100k, 1%
C30N 1.0uF, 25V, 20% X5R
R38N 10k, 1%
Q12N Si4435DY
Q13N 2N7002W

U14N APX803–44–SAG–7 or RT9818CXXGVL 4.2V–4.38V setpoint
GND, VCC, RESET
RESETBMCU
C33N 0.1uF, 25V, X5R
Reset monitor, PFUZE reset is too short



| | |
|---|---|
| Sheet: /U_05pwr_input/ | |
| File: 05pwr_input.sch | |
| **Title: 05pwr_input** | |
| Size: B | Date: 22 12 2014 |
| KiCad E.D.A. eeschema (2014–08–05 BZR 5054)–product | Rev: Id: 5/16 |

A, B, and C correspond to labelled jumpers below

| | BT_MD | | BT_CFG1 | | | | | | | | BT_CFG2 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit position | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Common bits | | | 0 | | | 0/PU | 0 | 0 | | 0 | 0 | 0 | 1 | | | 0 | 0 | 0 |
| serial vs. normal | A | A | | | | | | | | | | | | | | | | |
| SD vs. SATA | | | | B | B | | | | | | | | | | | | | |
| SD int. v ext | | | | | | | | | C | | | | | C | C | | | |

P_TAMPER

Male 2.54mm 2x1 right angle (DNP)

hard reset

TL3342F160QG/TR

SW10B

TL3342F160QG/TR (DNP)

SW11B

DNP; CPU power state controlled by charger board

NT10B

Heat sink Advanced Thermal Solutions ATS-56001-C3-R0

R17B 10k, 1%

C10B 0.1uF, 25V, X5R (DNP)

U100_4

iMX6Q - MCIMX6Q5EYM12AC

i.MX6Q - EIM

| | | |
|---|---|---|
| EIM_LBA | K22 | EIM_LBA |
| EIM_OE | J24 | EIM_OE |
| EIM_RW | K20 | EIM_RW |
| EIM_CS0 | H24 | EIM_CS0 |
| EIM_CS1 | J23 | EIM_CS1 |
| EIM_A16 | H25 | EIM_A16 |
| EIM_A17 | G24 | EIM_A17 |
| EIM_A18 | J22 | EIM_A18 |
| EIM_A19 | G25 | UIM_DATA |
| EIM_A20 | H22 | UIM_CLK |
| EIM_A21 | H23 | UIM_RESET |
| EIM_A22 | F24 | PCIE_WDIS_N |
| EIM_A23 | J21 | UIM_PWRON |
| EIM_A24 | F25 | HDMI_HPD_CPU |
| EIM_A25 | H19 | CEC |
| EIM_D16 | C25 | DDC_SDA |
| EIM_D17 | F21 | I2C3_SCL |
| EIM_D18 | D24 | I2C3_SDA |
| EIM_D19 | G21 | EPIT1_EPITO |
| EIM_D20 | G20 | EPIT2_EPITO |
| EIM_D21 | H20 | SMB_SCL |
| EIM_D22 | E23 | PCIE_WAKE |
| EIM_D23 | D25 | RGMII_NRST |
| EIM_D24 | F22 | UART3_TXD |
| EIM_D25 | G22 | UART3_RXD |
| EIM_D26 | E24 | UART2_TXD |
| EIM_D27 | E25 | UART2_RXD |
| EIM_D28 | G23 | SMB_SDA |
| EIM_D29 | J19 | PCIE_RST |
| EIM_D30 | J20 | SATA_PWRON |
| EIM_D31 | H21 | |
| EIM_EB2 | E22 | DDC_SCL |
| EIM_EB3 | F23 | |
| EIM_BCLK | N22 | EIM_BCLK |
| EIM_WAIT | M25 | EIM_WAIT |
| EIM_EB0 | K21 | |
| EIM_EB1 | K23 | |
| EIM_DA0 | L20 | EIM_DA0 |
| EIM_DA1 | J25 | EIM_DA1 |
| EIM_DA2 | L21 | EIM_DA2 |
| EIM_DA3 | K24 | EIM_DA3 |
| EIM_DA4 | L22 | EIM_DA4 |
| EIM_DA5 | L23 | EIM_DA5 |
| EIM_DA6 | K25 | EIM_DA6 |
| EIM_DA7 | L25 | EIM_DA7 |
| EIM_DA8 | L24 | EIM_DA8 |
| EIM_DA9 | M21 | EIM_DA9 |
| EIM_DA10 | M22 | EIM_DA10 |
| EIM_DA11 | M20 | EIM_DA11 |
| EIM_DA12 | M24 | EIM_DA12 |
| EIM_DA13 | M23 | EIM_DA13 |
| EIM_DA14 | N23 | EIM_DA14 |
| EIM_DA15 | N24 | EIM_DA15 |

NVCC_EIM1

NVCC_EIM0

NVCC_EIM2

note: SMB pins on this sheet are only used for D/Q config

R23B 10k, 1% (DNP)

R25B 10k, 1%

P_USB

2 pin 1.27mm male header

R27B 10k, 1%

R28B 100k, 1%

tamper detect

0 = disable tamper

Q10B 2N7002W

R29B 10k, 1%

header absent = boot from storage

header present = boot from USB

P_FUSE

2 pin 1.27mm male header

Y10B

24.0000 MHz 15ppm 8pF 70 ohm ESR (NDK NX3225SA)

R32B 10M, 1% (DNP)

R33B 2.2M, 1%

C11B 18pF, NPO

C12B 18pF, NPO

U100_3

iMX6Q - MCIMX6Q5EYM12AC

i.MX6Q - CONTROL

| | | |
|---|---|---|
| CPU_ONOFF | D12 | ONOFF |
| RESETBMCU | C11 | POR_B |
| CPU_BOOTMODE0 | C12 | BOOT_MODE0 |
| CPU_BOOTMODE1 | F12 | BOOT_MODE1 |
| CPU_TEST_MODE | E12 | TEST_MODE |
| CPU_TAMPER | E11 | TAMPER |
| PMIC_STBY_REQ | F11 | PMIC_STBY_REQ |
| PMIC_ON_REQ | D11 | PMIC_ON_REQ |
| CPU_XTALI | A7 | XTALI |
| CPU_XTALO | B7 | XTALO |
| RTC_XTALI | D9 | RTC_XTALI |
| RTC_XTALO | C9 | RTC_XTALO |

VDD_SNVS_IN

NVCC_JTAG

| | | |
|---|---|---|
| JTAG_TCK | H5 | |
| JTAG_TMS | C3 | |
| JTAG_TDI | G5 | |
| JTAG_TDO | G6 | |
| JTAG_TRSTB | C2 | |
| JTAG_MOD | H6 | |
| CLK1_N | C7 | |
| CLK1_P | D7 | |
| CLK2_N | C5 | CLK2_N |
| CLK2_P | D5 | CLK2_P |

R14B 10k, 1%

R15B 10k, 1%

R16B 10k, 1%

R13B 100, 1%

P10B

Male 2.54mm 8x2 header (DNP)

JTAG_TRST

JTAG_TDI

JTAG_TMS

JTAG_TCK

JTAG_RTCK

JTAG_TDO

JTAG_NRST

RESETBMCU R18B 0 ohm

R19B 10k, 1%

R20B 1k, 1%

R22B 10k, 1% (DNP)

R26B 4.7k, 1%

DIFFPAIR_PCIE_REFCLK_N

DIFFPAIR_PCIE_REFCLK_P

PCIE_CLK

DIFFPAIR

R57B 100, 1% (DNP)

DIFFPAIR

C10B 0.1uF, 25V, X5R (DNP)

RTC_XTALO

R34B 10M, 1% (DNP)

Abracon ABS06-32.768KHZ-T 12.5pF CL

Y11B

C13B 18pF, NPO

C14B 18pF, NPO

Default boot: internal microSD

Boot select header precedence: P_USB (A) > P_SATA (B) > PEXT (C)

P_FUSE must be used alone, if at all

R35B 10k, 1%

R36B 0 ohm (DNP)

R37B 4.7k, 1%

BT_CFG1_1

R38B 4.7k, 1%

BT_CFG1_5

R40B 4.7k, 1%

BT_CFG1_6

R42B 4.7k, 1%

BT_CFG2_3

R44B 4.7k, 1%

BT_CFG2_4

R46B R47B R48B R49B R50B R51B R52B R53B R54B R55B 10k, 1%

BOOT_CFG1[7:0]: 0XX0 00X0

BOOT_CFG2[7:0]: 001X X000

P_SATA

2 pin 1.27mm male header

R43B 10k, 1%

BT_CFG1_6

BT_CFG1_5

Q13B 2N7002W

header absent = boot from SD

header present = boot from SATA

R56B 10k, 1%

BT_CFG1_6 = !BT_CFG1_5

P_EXT

2 pin 1.27mm male header

R41B 10k, 1%

BT_CFG1_1 <- replicate to isolate BT_CFG2_4

BT_CFG2_3

Q11B 2N7002W

R45B 10k, 1%

Q12B 2N7002W

R39B 10k, 1%

header absent = boot from internal SD

header present = boot from external SD

BT_CFG1_1 = !BT_CFG2_3

BT_CFG2_4 = !BT_CFG2_3



Sheet: /U_06cpu_soc/

File: 06cpu_soc.sch

Title: 06cpu_soc

Version: PVT2-A

Size: B | Date: 22 12 2014 | Rev:

KiCad E.D.A. eeschema (2014-08-05 BZR 5054)-product | Id: 6/16

## Internal microSD card (main boot)

R10S 1k, 1%
C10S 0.01uF, 10V, X5R, 10%
R12S 100k, 1%
Q10S 2N7002W
R11S 68k, 1%
SD3_RST_N
SD3_RST_INV
Q11S FDN304P
support 200mA max SDCARD_VDD
C11S 4.7uF, 10V, X5R, 10%
C12S 0.1uF, 6.3V, X5R
R13S 100, 1%
Q12S 2N7002W
R14S 10k, 1%
J10S AUK TFC08W01-HC-H
DAT2 SD3_DAT2
CD/DAT3 SD3_DAT3
CMD SD3_CMD
VDD
CLK SD3_CLK
VSS
DAT0 SD3_DAT0
DAT1 SD3_DAT1
NT11S Novena PVT1 firmware
NT10S 4 GByte MicroSD (Sandisk SDSDQ-4096)
ensure low voltage for proper reset

## External SD card

JP10S SD/MMC HRS DM1AA-SF-PEJ(21)
DAT3/RSV SD2_DAT3
CMD SD2_CMD
GND
VCC
CLK SD2_CLK
GND
DAT0/DAT SD2_DAT0
DAT1 SD2_DAT1
DAT2 SD2_DAT2
WP SD2_WP
CD_WP_COM CD_W
CD SD2_CD
CASE
R17S 10k, 1%
R18S 10k, 1%
R19S 10k, 1%
C13S 0.1uF, 6.3V, X5R

## Utility EEPROM, 64kx8

Store non-volatile configuration info
And possibly parts of panic logs
U10S FT24C512AUTR-T
A0 VCC
A1 WP
A2 SCL I2C3_SCL
GND SDA I2C3_SDA
C14S 0.1uF, 6.3V, X5R
Device addr = 0xAC

## U100_5 iMX6Q – MCIMX6Q5EYM12AC

i.MX6Q

GPT_CMPOUT1 B21 SD1_CMD
GPT_CLKIN D20 SD1_CLK
GPT_CAPIN1 A21 SD1_DAT0
FPGA_EXP_ON C20 SD1_DAT1
E19 SD1_DAT2
GPT_CMPOUT3 F18 SD1_DAT3
NVCC_SD1

SD2_CMD F19 SD2_CMD
SD2_CLK C21 SD2_CLK
SD2_DAT0 A22 SD2_DAT0
SD2_DAT1 E20 SD2_DAT1
SD2_DAT2 A23 SD2_DAT2
SD2_DAT3 B22 SD2_DAT3
NVCC_SD2

SD3_CMD B13 SD3_CMD
SD3_CLK D14 SD3_CLK
SD3_DAT0 E14 SD3_DAT0
SD3_DAT1 F14 SD3_DAT1
SD3_DAT2 A15 SD3_DAT2
SD3_DAT3 B15 SD3_DAT3
D13 SD3_DAT4
C13 SD3_DAT5
E13 SD3_DAT6
F13 SD3_DAT7
SD3_RST_N D15 SD3_RST
NVCC_SD3

B11 MLB_CP
A11 MLB_CN
B9 MLB_SP
A9 MLB_SN
A10 MLB_DP
B10 MLB_DN

ENET_MDC V20 RGMII_MDC
ENET_MDIO V23 RGMII_MDIO
ENET_CRS_DV U21
ENET_REF_CLK V22 RGMII_REF_CLK
ENET_RX_ER W23 OTG_ID
ENET_TX_EN V21 RGMII_INT
ENET_RXD0 W21
ENET_RXD1 W22
ENET_TXD0 U20
ENET_TXD1 W20
NVCC_ENET

KEY_COL0 W5 UART4_TXD
KEY_ROW0 V6 UART4_RXD
KEY_COL1 U7 KEY_COL1
KEY_ROW1 U6 KEY_ROW1
KEY_COL2 W6 KEY_COL2
KEY_ROW2 W4 KEY_ROW2
KEY_COL3 U5 KEY_COL3
KEY_ROW3 T7 KEY_ROW3
KEY_COL4 T6 KEY_COL4
KEY_ROW4 V5 LCD_BL_ON

GPIO_0 T5 AUD_MCLK_T
GPIO_1 T4
GPIO_2 T1 SD2_WP
GPIO_3 R7
GPIO_4 R6 SD2_CD
GPIO_5 R4
GPIO_6 T3
GPIO_7 R3
GPIO_8 R5
GPIO_9 T2
GPIO_16 R2
GPIO_17 R1 PCIE_PWRON
GPIO_18 P6
GPIO_19 P5 RGMII_INT
NVCC_GPIO

NANDF_CS0 F15
NANDF_CS1 C16
NANDF_CS2 A17
NANDF_CS3 D16
NANDF_ALE A16
NANDF_CLE C15
NANDF_WP_B E15
NANDF_RB0 B16
NANDF_D0 A18
NANDF_D1 C17
NANDF_D2 F16
NANDF_D3 D17
NANDF_D4 A19
NANDF_D5 B18
NANDF_D6 F17
NANDF_D7 C18
SD4_CLK E16
SD4_CMD B17
SD4_DAT0 D18
SD4_DAT1 B19
SD4_DAT2 F17
SD4_DAT3 A20
SD4_DAT4 E18
SD4_DAT5 C19
SD4_DAT6 B20
SD4_DAT7 D19
NVCC_NANDF

R21S 300, 1%
R20S 49.9, 1% (DNP)
C16S 2200pF, X7R, 50V, 10% (DNP)
note: this is a high speed line at 125 MHz, route as 50 ohms
note double-up on this pin
ambiguous if one is better than the other, but no harm to wire up both
(one BSP uses P5, another uses V21)
DQ only
R15S 10k, 1%
C15S 0.1uF, 6.3V, X5R
TL3342F160QG/TR SW10S
TL3342F160QG/TR (DNP) SW11S
Place mirror-image on bottom side of board
AUD_CLK
close to CPU
R16S 49.9, 1%
AUD_MCLK
AUD_CLK
50 ohm trace



Sheet: /U_07sdcard/
File: 07sdcard.sch
Title: 07sdcard
Kosagi PVT2-A
Size: B | Date: 22 12 2014 | Rev:
KiCad E.D.A. eeschema (2014-08-05 BZR 5054)-product | Id: 7/16

## OTG port – allow B mode only

Micro-B
P10U
FCI 10103594-0001LF
VBUS
D–
D+
ID
GND
PAD
OTG_VBUS
USB_OTG_N
USB_OTG_P
OTG_ID
R41U
R42U
100k, 1%
RCLAMP0502B
D10U
RSA5M
C21U
0.1uF, 25V, X5R
C25U
R20U
100, 1%
D15U
RSA5M

## SoC interface

U100_6
iMX6Q – MCIMX6Q5EYM12AC
i.MX6Q – USB
USB_OTG_CHD_B
USB_OTG_VBUS
USB_OTG_DN
USB_OTG_DP
VDDUSB_CAP
USB_H1_DP
USB_H1_DN
USB_H1_VBUS
OTG_VBUS
R43U
0 ohm
USB_VBUS
R25U
0 ohm
C24U
C35U
4.7uF, 10V, X5R 10%
0.22uF, 6.3V, X5R 10%
C33U
C34U
10uF, 10V, X5R, 20%
USB_OTG_N
USB_OTG_P
USB_H1_D_P
USB_H1_D_N
VBUS_HOST
C36U
C27U
4.7uF, 10V, X5R, 10%

## Primary function hub

U10U
GL852GCG-QFP48
R10U
0 ohm (DNP)
C10U
4.7uF, 10V, X5R, 10% (DNP)
R13U
0 ohm (DNP)
C11U
10uF, 10V, X5R, 20% (DNP)
R12U
10k, 1%
R11U
100k, 1%
set for individual power management
R14U
10k, 1%
USB_PWREN1_N
USB_OVERCUR1_N
internal pullup
self-powered
L10U
BLM18KG121
3A 120 ohm
USB_P3.3VA
C12U
C13U
C14U
C15U
C16U
C17U
C18U
0.1uF, 6.3V, X5R
4.7uF, 10V
R15U
10k, 1%
U11U
RT9711BGB
FLG
GND
EN
VOUT
VIN
C22U
1.0uF, 25V, 20%
L11U
BLM18KG121
3A 120 ohm
D16U
RSA5M
P5.0V_USBEXT1
P11U
AUK USB-1X04-SR-BK-S-H
C23U
0.1uF, 25V, X5R
USB_NETS
DIFFPAIR
RCLAMP0502B
Amber1/Green4 NC => Port 1 is CDP
USB_H1_D_N
USB_H1_D_P
USB_EXT1_N
USB_EXT1_P
USB_ETH_N
USB_ETH_P
use explicit reset line to reboot USB ethernet
USB ethernet has no power control
R22U
680, 1%
C20U
C19U
ports 2/3 are non-removable
R17U
R18U
R16U
R19U
10k, 1%
low-active power switches
USB_PWREN3_N
USB_OVERCUR3_N
internal pullup
R21U
10k, 1%
MASTERHUB_RESET
R23U
0 ohm
RESETBMCU
R27U
0 ohm (DNP)
USB_HUB1_RST
R26U
1k, 1%
R24U
10k, 1%
AMBER3/4 PD => 4 DP declared
USB_NETSUSB_OPT_NDIFFPAIR1
USB_NETSUSB_OPT_PDIFFPAIR1
USB_NETSUSB_OPT_NDIFFPAIR2
USB_NETSUSB_OPT_PDIFFPAIR2
USB_NETSUSB_PCI_N DIFFPAIR
USB_NETSUSB_PCI_P DIFFPAIR
Y10U
12.0000 MHz (NDK NX5032GB-12MHZ-STD-CSK-5, 30ppm, 8pF)
C31U
C32U
8.2 pF, NP0

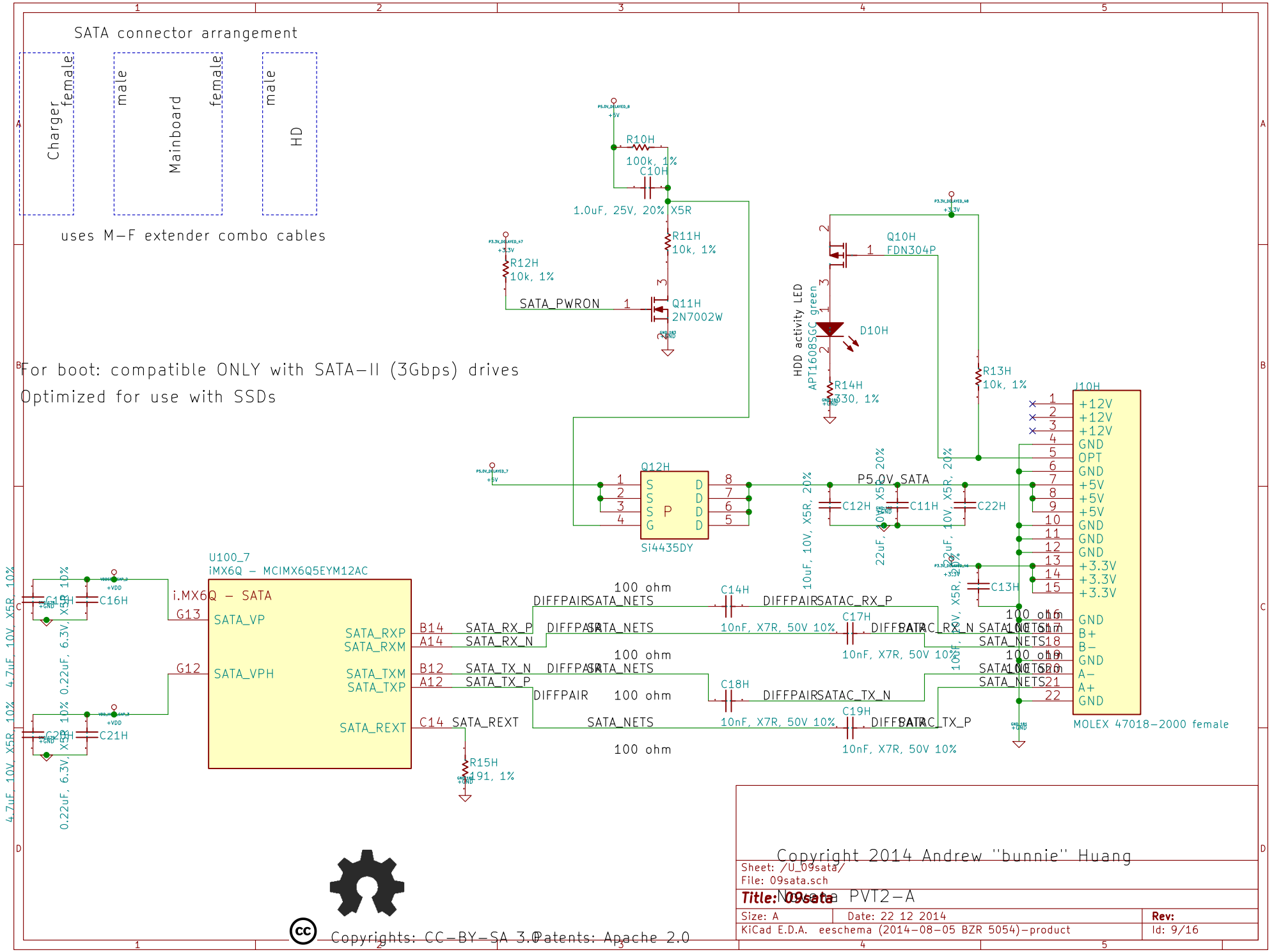
## Slave function hub

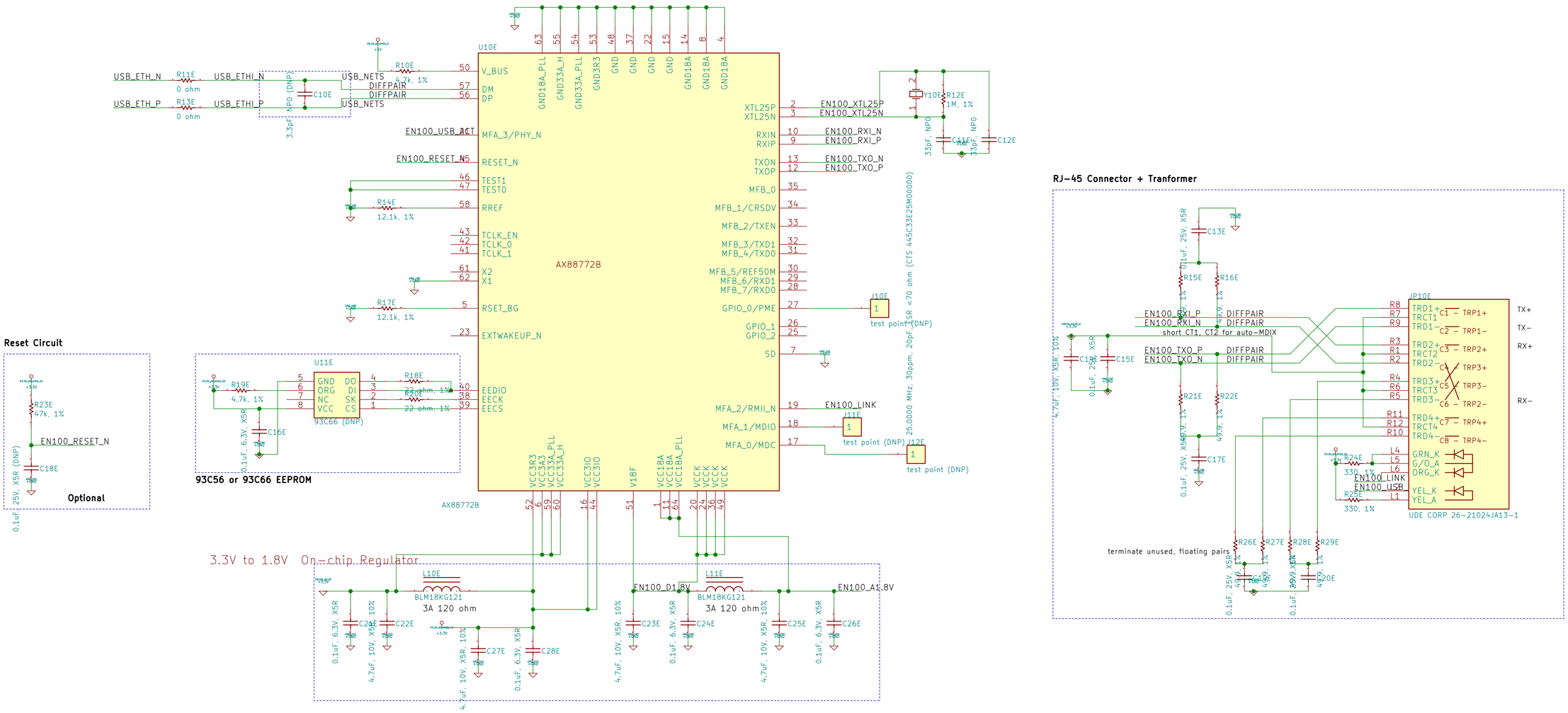
U13U
GL852GCG-QFP48
R28U
0 ohm (DNP)
C37U
4.7uF, 10V, X5R, 10% (DNP)
R31U
0 ohm (DNP)
C38U
10uF, 10V, X5R, 20% (DNP)
R30U
10k, 1%
R29U
100k, 1%
set for individual power management
R32U
10k, 1%
Amber1/Green4 NC => Port 1 is CDP
self-powered
L13U
BLM18KG121
3A 120 ohm
USB_P3.3VB
C39U
C40U
C41U
C42U
C43U
C44U
C45U
C47U
R33U
10k, 1%
U14U
RT9711BGB
USB_OVERCUR8_N
USB_PWREN8_N
C48U
1.0uF, 25V, 20%
L14U
BLM18KG121
3A 120 ohm
D17U
RSA5M
P5.0V_USBEXT2
P13U
AUK USB-1X04-SR-BK-S-H
C49U
0.1uF, 25V, X5R
USB_EXT2_N
USB_EXT2_P
RCLAMP0502B
USB_OPT_N
USB_OPT_P
USB_MOUSE_N
USB_MOUSE_P
R37U
680, 1%
R34U
R35U
10k, 1%
low-active power switches
USB_PWREN7_N
USB_OVERCUR7_N
USB_PWREN8_N
USB_OVERCUR8_N
SLAVEHUB_RESET
R36U
10k, 1%
R44U
0 ohm
RESETBMCU
R46U
0 ohm (DNP)
USB_HUB2_RST
R45U
1k, 1%
R38U
10k, 1%
Amber1/Green4 NC => Port 1 is CDP
AMBER3/4 PD => 4 DP declared
USB_NETSUSB_KBD_NDIFFPAIR7
USB_NETSUSB_KBD_PDIFFPAIR7
USB_NETSUSB_KBD_NDIFFPAIR8
USB_NETSUSB_KBD_PDIFFPAIR8
USB_NETSUSB_VID_NDIFFPAIR21
USB_NETSUSB_VID_PDIFFPAIR21
USB_NETSUSB_VID_NDIFFPAIR22
USB_NETSUSB_VID_PDIFFPAIR22
Y11U
12.0000 MHz (NDK NX5032GB-12MHZ-STD-CSK-5, 30ppm, 8pF)
C53U
C54U
8.2 pF, NP0

U15U
RT9706
VIN
EN
GND
VOUT
FLG
USB_PWREN6_N
P5.0V_MOUSE
USB_OVERCUR6_N
R39U
10k, 1%
R40U
10k, 1%
C51U
10uF, 10V, X5R, 20%
U16U
RT9706
USB_PWREN7_N
P5.0V_KBD
USB_OVERCUR7_N
C55U
C56U
1.0uF, 25V, 20% X5R
C52U
to front panel USB breakout via 30-pin FFC



| | |
|---|---|
| Sheet: /U_08usb/ | |
| File: 08usb.sch | Novena PVT2-A |
| **Title: 08usb** | |
| Size: C | Date: 22 12 2014 |
| KiCad E.D.A. | eeschema (2014-08-05 BZR 5054)-product |
| **Rev:** | Id: 8/16 |


SATA connector arrangement
Charger
female
male
Mainboard
female
male
HD
uses M–F extender combo cables
For boot: compatible ONLY with SATA–II (3Gbps) drives
Optimized for use with SSDs
R10H
100k, 1%
C10H
1.0uF, 25V, 20% X5R
R11H
10k, 1%
R12H
10k, 1%
SATA_PWRON
Q11H
2N7002W
Q10H
FDN304P
D10H
HDD activity LED
APT1608SGC green
R14H
330, 1%
R13H
10k, 1%
J10H
MOLEX 47018–2000 female
Q12H
Si4435DY
P5.0V_SATA
C12H
C11H
C22H
C13H
U100_7
iMX6Q – MCIMX6Q5EYM12AC
i.MX6Q – SATA
SATA_VP
SATA_VPH
SATA_RXP
SATA_RXM
SATA_TXM
SATA_TXP
SATA_REXT
G13
G12
B14 SATA_RX_P
A14 SATA_RX_N
B12 SATA_TX_N
A12 SATA_TX_P
C14 SATA_REXT
R15H
191, 1%
C14H
C17H
C18H
C19H
10nF, X7R, 50V 10%
100 ohm
DIFFPAIR
SATA_NETS
SATAC_RX_P
SATAC_RX_N
SATAC_TX_N
SATAC_TX_P
C16H
C21H
4.7uF, 10V, X5R, 10%
0.22uF, 6.3V, X5R, 10%
Copyright 2014 Andrew "bunnie" Huang
Sheet: /U_09sata/
File: 09sata.sch
Title: 09sata PVT2–A
Size: A
Date: 22 12 2014
Rev:
KiCad E.D.A. eeschema (2014–08–05 BZR 5054)–product
Id: 9/16
Copyrights: CC–BY–SA 3.0 Patents: Apache 2.0








Novena PVT2-A

Sheet: /U_10ethernet100/
File: 10ethernet100.sch

**Title: 10ethernet100**

| Size: C | Date: 22 12 2014 | Rev: |
|---|---|---|
| KiCad E.D.A. eeschema (2014-08-05 BZR 5054)-product | | Id: 10/16 |

37 mA from P2.5V_VGEN5

563 mA DVDDL (1.2V)

75 mA AVDDH (3.3V)

25.0000 MHz, 30ppm, 20pF, ESR <70 ohm (CTS 445C33E25M00000)

3A 120 ohm

3A 120 ohm

U10G
KSZ9021RN

U100_8
i.MX6Q – RGMII
iMX6Q – MCIMX6Q5EYM12AC

U11G
LMR10510YSD

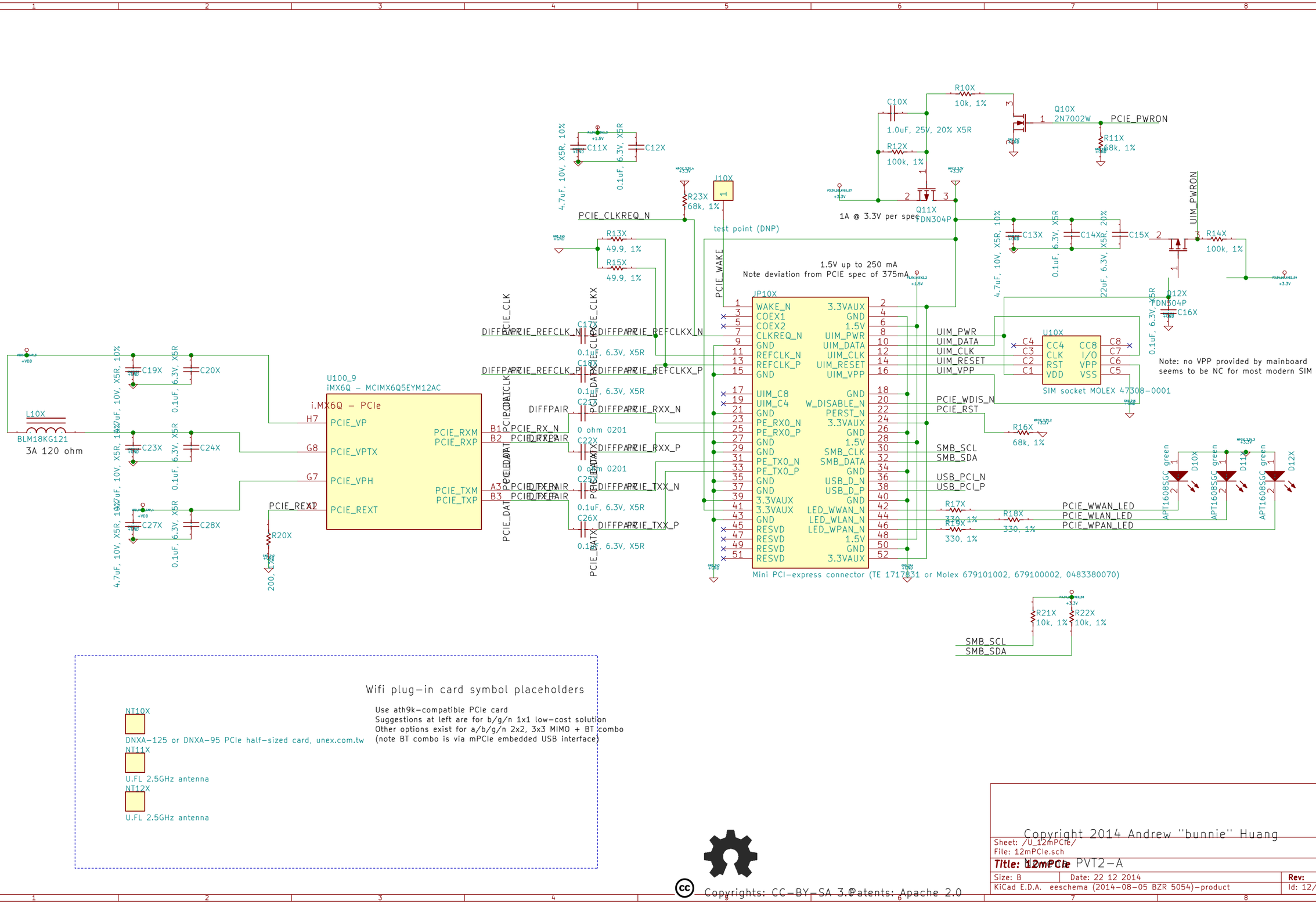
JP10G
UDE CORP 26-21024JA13-1



Sheet: /U_11ethernetGbit/
File: 11ethernetGbit.sch

**Title:** 11ethernetGbit

| Size: B | Date: 22 12 2014 | Rev: |
|---|---|---|
| KiCad E.D.A. eeschema (2014-08-05 BZR 5054)-product | | Id: 11/16 |






| | | |
|---|---|---|
| Sheet: /U_12mPCIe/ | | |
| File: 12mPCIe.sch | | |
| **Title: 12mPCIe** PVT2-A | | |
| Size: B | Date: 22 12 2014 | **Rev:** |
| KiCad E.D.A. eeschema (2014-08-05 BZR 5054)-product | | Id: 12/16 |

## LCD interface

Designed to work with LED backlight panels
Interleaved pixel option to support UXGA resolutions
Requires custom cable to adapt pinout to specific LCD

U100_10
iMX6Q – MCIMX6Q5EYM12AC
i.MX6Q – DISP: CSI

i.MX6 S/DL has AUD_MCLK on P3
AUD_MCLK — R26L 49.9, 1% (DNP) — AUD_MCLK_T_SDE
I11L test point (DNP)
AUD_CLK — R10L 49.9, 1% — AUD_CLK_T

| | | | |
|---|---|---|---|
| P4 | CSI0_MCLK | | |
| P1 | CSI0_PIXCLK | | |
| N2 | CSI0_VSYNC | BATT_NRST | |
| P3 | CSI0_DATA_EN | BATT_REFLASH_ALRT | |
| N1 | CSI0_DAT4 | AUD_CLK_T | |
| P2 | CSI0_DAT5 | AUD_DOUT | |
| N4 | CSI0_DAT6 | AUD_LRCLK | |
| N3 | CSI0_DAT7 | AUD_DIN | |
| N6 | CSI0_DAT8 | SMB_SDA | These are alt pins used only on SMB |
| N5 | CSI0_DAT9 | SMB_SCL | |
| M1 | CSI0_DAT10 | LCD_PWR_CTL | |
| M3 | CSI0_DAT11 | AUD_ALRCK | |
| M2 | CSI0_DAT12 | UART4_TXD | These are alt pins used only on SMB |
| L1 | CSI0_DAT13 | UART4_RXD | |
| M4 | CSI0_DAT14 | | |
| M5 | CSI0_DAT15 | | |
| L4 | CSI0_DAT16 | UART4_RTS | |
| L3 | CSI0_DAT17 | UART4_CTS | |
| M6 | CSI0_DAT18 | | |
| L6 | CSI0_DAT19 | | |

NVCC_CSI

| | | |
|---|---|---|
| F4 | CSI_CLK0M | |
| F3 | CSI_CLK0P | |
| E4 | CSI_D0M | |
| E3 | CSI_D0P | |
| D1 | CSI_D1M | |
| D2 | CSI_D1P | |
| E1 | CSI_D2M | |
| E2 | CSI_D2P | |
| F2 | CSI_D3M | |
| F1 | CSI_D3P | |
| D4 | CSI_REXT | CSI_REXT |

NVCC_MIPI

R13L 6.04k, 1%

| | | | |
|---|---|---|---|
| N19 | DIO_DISP_CLK | | |
| N25 | DIO_PIN2 | AUD6_TXD | |
| N20 | DIO_PIN3 | AUD6_TFS | |
| P25 | DIO_PIN4 | USB_HUB1_RST | AUD6_RXD |
| N21 | DIO_PIN15 | AUD6_TXC | |
| P24 | DISP0_DAT0 | ECSPI3_SCLK | |
| P22 | DISP0_DAT1 | ECSPI3_MOSI | |
| P23 | DISP0_DAT2 | ECSPI3_MISO | |
| P21 | DISP0_DAT3 | ECSPI3_SS0 | |
| P20 | DISP0_DAT4 | ECSPI3_SS1 | |
| R25 | DISP0_DAT5 | ECSPI3_SS2 | |
| R23 | DISP0_DAT6 | USB_HUB2_RST | AUD6_RXC |
| R24 | DISP0_DAT7 | ECSPI3_RDY | |
| R22 | DISP0_DAT8 | GPIO_PWM1 | |
| T25 | DISP0_DAT9 | GPIO_PWM2 | |
| R21 | DISP0_DAT10 | FPGA_SUSPEND | |
| T23 | DISP0_DAT11 | FPGA_INIT_N | |
| T24 | DISP0_DAT12 | FPGA_DONE | |
| R20 | DISP0_DAT13 | FPGA_RESET_N | |
| U25 | DISP0_DAT14 | FPGA_TCK | |
| T22 | DISP0_DAT15 | FPGA_TDI | |
| T21 | DISP0_DAT16 | FPGA_TDO | |
| U24 | DISP0_DAT17 | FPGA_TMS | |
| V25 | DISP0_DAT18 | ACCEL_INT | |
| U23 | DISP0_DAT19 | TS_TOUCHED | |
| U22 | DISP0_DAT20 | PCIE_CLKREQ_N | |
| T20 | DISP0_DAT21 | AUD_HP_IN | |
| V24 | DISP0_DAT22 | PMIC_INT_B | |
| W24 | DISP0_DAT23 | AUD_PWRON | |

NVCC_LCD

| | | |
|---|---|---|
| H3 | DSI_CLK0M | |
| H4 | DSI_CLK0P | |
| G2 | DSI_D0M | |
| G1 | DSI_D0P | |
| H2 | DSI_D1M | |
| H1 | DSI_D1P | |
| G4 | DSI_REXT | DSI_REXT |

NVCC_MIPI

R14L 6.04k, 1%

HUB RST normally DNP, so available to talk to FPGA

U100_11
iMX6Q – MCIMX6Q5EYM12AC
i.MX6Q – LVDS

| | | | |
|---|---|---|---|
| U2 | LVDS0_TX0_N | LVDS0_TX_0_N | DIFFPAIR |
| U1 | LVDS0_TX0_P | LVDS0_TX_0_P | DIFFPAIR |
| U4 | LVDS0_TX1_N | LVDS0_TX_1_N | DIFFPAIR |
| U3 | LVDS0_TX1_P | LVDS0_TX_1_P | DIFFPAIR |
| V2 | LVDS0_TX2_N | LVDS0_TX_2_N | DIFFPAIR |
| V1 | LVDS0_TX2_P | LVDS0_TX_2_P | DIFFPAIR |
| V4 | LVDS0_CLK_N | LVDS0_CLK_N | DIFFPAIR |
| V3 | LVDS0_CLK_P | LVDS0_CLK_P | DIFFPAIR |
| W2 | LVDS0_TX3_N | LVDS0_TX_3_N | DIFFPAIR |
| W1 | LVDS0_TX3_P | LVDS0_TX_3_P | DIFFPAIR |
| V7 | NVCC_LVDS2P5 | | |
| Y1 | LVDS1_TX0_N | LVDS1_TX0_N | DIFFPAIR |
| Y2 | LVDS1_TX0_P | LVDS1_TX0_P | DIFFPAIR |
| AA2 | LVDS1_TX1_N | LVDS1_TX1_N | DIFFPAIR |
| AA1 | LVDS1_TX1_P | LVDS1_TX1_P | DIFFPAIR |
| AB1 | LVDS1_TX2_N | LVDS1_TX2_N | DIFFPAIR |
| AB2 | LVDS1_TX2_P | LVDS1_TX2_P | DIFFPAIR |
| Y3 | LVDS1_CLK_N | LVDS1_CLK_N | DIFFPAIR |
| Y4 | LVDS1_CLK_P | LVDS1_CLK_P | DIFFPAIR |
| AA3 | LVDS1_TX3_N | LVDS1_TX_3_N | DIFFPAIR |
| AA4 | LVDS1_TX3_P | LVDS1_TX_3_P | DIFFPAIR |

NVCC_LVDS2P5

C11L 0.1uF, 6.3V, X5R

0.5A / contact
4x for LCD digital logic (2A max)
5x for BL (2.5A x Vbat watts)

JP10L

| | | | |
|---|---|---|---|
| 1 | LCD_XP | | |
| 2 | LCD_YP | | |
| 3 | LCD_XM | | |
| 4 | LCD_YM | | |
| 5 | GPIO_PWM1 | | |
| 6 | LCD_BL_ON | | |
| 7 | I2C3_SCL | | |
| 8 | I2C3_SDA | | |
| 9 | | | |
| 10 | LVDS0_TX_0_N | | |
| 11 | LVDS0_TX_0_P | | |
| 12 | | | |
| 13 | LVDS0_TX_1_N | | |
| 14 | LVDS0_TX_1_P | | |
| 15 | | | |
| 16 | LVDS0_TX_2_N | | |
| 17 | LVDS0_TX_2_P | | |
| 18 | | | |
| 19 | LVDS0_CLK_N | | |
| 20 | LVDS0_CLK_P | | |
| 21 | | | |
| 22 | LVDS0_TX_3_N | | |
| 23 | LVDS0_TX_3_P | | |
| 24 | | | |
| 25 | LVDS1_TX0_N | | |
| 26 | LVDS1_TX0_P | | |
| 27 | | | |
| 28 | LVDS1_TX1_N | | |
| 29 | LVDS1_TX1_P | | |
| 30 | | | |
| 31 | LVDS1_TX2_N | | |
| 32 | LVDS1_TX2_P | | |
| 33 | | | |
| 34 | LVDS1_CLK_N | | |
| 35 | LVDS1_CLK_P | | |
| 36 | | | |
| 37 | LVDS1_TX_3_N | | |
| 38 | LVDS1_TX_3_P | | |
| 39 | | | |
| 40 | combo logic+EDID power | | |
| 41 | LCD_VCC_SW | | |
| 42 | | | |
| 43 | | | |
| 44 | | | |
| 45 | | | |
| 46 | USB_VID_P5V | | |
| 47 | USB_VID_N | | |
| 48 | USB_VID_P | | |
| 49 | | | |
| 50 | | | |
| 51 | | | |
| 52 | | | |
| 53 | backlight power | | |
| 54 | LCD_BL_VDD | | |

54-pin FFC MOLEX 51296-5494 or equiv

LCD_VCC leads LCD_BL voltages in power-on and down transitions

Q10L SI4435DY
R11L 100k, 1%
C14L 1.0uF, 25V, 20% X5R
LCD_VCC_SW
C12L 4.7uF, 10V, X5R, 10%
C13L 0.1uF, 6.3V, X5R

R15L 10k, 1%
LCD_PWR_CTL — R18L 100k, 1% — Q12L 2N7002W
R17L 49.9, 1%
Q13L 2N7002W

voltage range compatible with most LED backlit displays

BATT_PWR
Q11L SI4435DY
R16L 10k, 1%
C19L 1.0uF, 25V, 20% X5R
LCD_BL_VDD
C17L 0.1uF, 25V, X5R
C18L 22uF, 25V, X5R, 10%
R19L 10k, 1%
R16L, R19L must divide BATT_PWR to protect Si4435DY 20V Vgs
Also means BATT_PWR > 6V to turn-on transistor
Q14L 2N7002W

active pull-down in off state
to ensure LCD circuitry reset

U10L
RT9706
USB_PWREN5_N
C15L 1.0uF, 25V, 20% X5R
USB_VID_P5V
C16L 10uF 10V, X5R, 20%
USB_OVERCUR5_N
R12L 10k, 1%

## HDMI ESD

D10L D11L D12L
RCLAMP0524P

| | | | |
|---|---|---|---|
| | CEC | CEC | |
| | DDC_SCL_HV | DDC_SCL_HV | |
| | GND1 | | |
| | DDC_SDA_HV | DDC_SDA_HV | |
| | HDMI_HPD | HDMI_HPD | |
| | PCB Rule TX0_TMDS3_N | TX0_TMDS3_N | PCB Rule |
| | TX0_TMDS3_P | TX0_TMDS3_P | |
| | Matched Net Lengths [Tolerance = 10mil] | | Matched Net Lengths [Tolerance = 2mil] |
| | GND1 | | |
| | TX0_TMDS0_N | TX0_TMDS0_N | |
| | TX0_TMDS0_P | TX0_TMDS0_P | |
| | TX0_TMDS1_N | TX0_TMDS1_N | |
| | TX0_TMDS1_P | TX0_TMDS1_P | |
| | GND1 | | |
| | TX0_TMDS2_N | TX0_TMDS2_N | |
| | TX0_TMDS2_P | TX0_TMDS2_P | PCB Rule |

Matched Net Lengths [Tolerance = 4mil]

U100_12
iMX6Q – MCIMX6Q5EYM12AC
i.MX6Q – HDMI

| | | |
|---|---|---|
| K1 | HDMI_HPD | HDMI_HPD_CPU |
| K2 | HDMI_DDCCEC | |
| L7 | HDMI_VP | |
| M7 | HDMI_VPH | |
| J5 | HDMI_CLKM | |
| J6 | HDMI_CLKP | |
| K5 | HDMI_D0M | |
| K6 | HDMI_D0P | |
| J3 | HDMI_D1M | |
| J4 | HDMI_D1P | |
| K3 | HDMI_D2M | |
| K4 | HDMI_D2P | |
| F1 | HDMI_REF | |

C20L C21L C22L C23L 4.7uF, 10V, X5R, 10%
0.1uF, 6.3V, X5R
HDMI_REF — R24L 1.6k, 1%

LAYOUT: PLACE ESD IN SERIES TO ELIMINATE STUBS
RUN TRACES STRAIGHT UNDER ESD WITHOUT VIAS

LAYOUT: ROUTE HDMI_TX* AND TX* SHORT, STRAIGHT,
AND WITHOUT VIAS. ROUTE PAIRS WITH
100 OHM DIFFERENTIAL IMPEDANCE.

Note leakage point on 3.3V line
(but, buffer prevents trivial attack on PMIC from HDMI port)

R33L 4.7k, 1%
Q19L BSS138
DDC_SCL — R20L 1.8k, 1% — Q15L BSS138

Use P3.3V for P/Us because DDC lines are shared with PMIC lines
(why this is recommended by Freescale, I don't know)

C10L 0.1uF, 6.3V, X5R
R21L 1.8k, 1%
R22L 1.8k, 1%
R23L 1.8k, 1%
DDC_SDA — Q16L BSS138
can't use 2N7002 here b/c Vth is too high

HDMI_HPD_CPU
R27L 0 ohm
R28L 0 ohm (DNP)

R29L 1k, 1%
R30L 10k, 1%
HDMI_HPD_LV — Q17L 2N7002W
HDMI_HPD_LV_N — Q18L 2N7002W — HDMI_HPD

No HPD polarity select in software
So, hardware buffering required

## HDMI-A connector

Matched Net Lengths [Tolerance = 2mil]
PCB Rule

J10L

| | | | |
|---|---|---|---|
| 1 | HDMI_TX | TX0_TMDS2_P | DIFFPAIR |
| 2 | HDMI_TX | TX0_TMDS2_N | DIFFPAIR |
| 3 | HDMI_TX | TX0_TMDS1_P | DIFFPAIR |
| 4 | | | |
| 5 | HDMI_TX | TX0_TMDS1_N | DIFFPAIR |
| 6 | HDMI_TX | TX0_TMDS0_P | DIFFPAIR |
| 7 | | | |
| 8 | HDMI_TX | TX0_TMDS0_N | DIFFPAIR |
| 9 | HDMI_TX | TX0_TMDS3_P | DIFFPAIR |
| 10 | | | |
| 11 | HDMI_TX | TX0_TMDS3_N | DIFFPAIR |
| 12 | CEC | R31L 100, 1% | |
| 13 | | | |
| 14 | DDC_SCL_HV | | |
| 15 | DDC_SDA_HV | | |
| 16 | | | |
| 17 | TX_HDMI_5V | | |
| 18 | HDMI_HPD | R32L 330, 1% | |
| 19 | | | |
| GND | | | |

AUK HDM19SW-4-L2-1R3HHCN

R25L 47k, 1%

## HDMI +5V fuse

F10L 0ZCA0005FF2E
INFO: 50MA hold
150MA TRIP
D13L RSA5M



Sheet: /U_13hdmi_lcd/
File: 13hdmi_lcd.sch
Nevena PVT2-A
**Title: 13hdmi_lcd**

| | | |
|---|---|---|
| Size: C | Date: 22 12 2014 | **Rev:** |
| KiCad E.D.A. | eeschema (2014-08-05 BZR 5054)-product | Id: 13/16 |

Microphone configured for pseudo-differential operation

note: reprogram in BSP to 3.0V for micbias use, in case AUD_P3.3V is too noisy

Note: TS4990IST can be substituted for NS4890

Power management switch for audio circuit

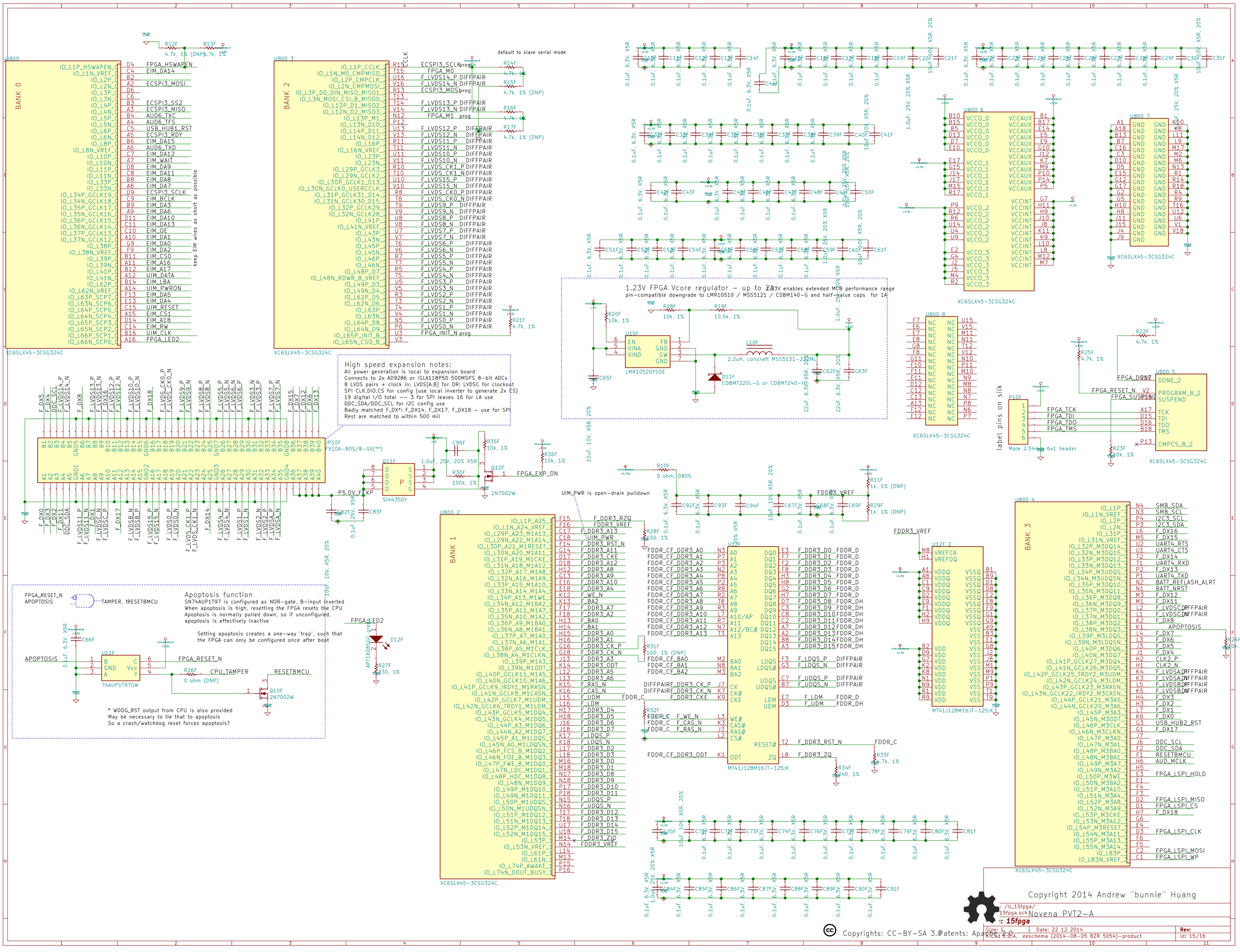
active pulldown
to ensure audio codec reset



Sheet: /U_14audio/
File: 14audio.sch

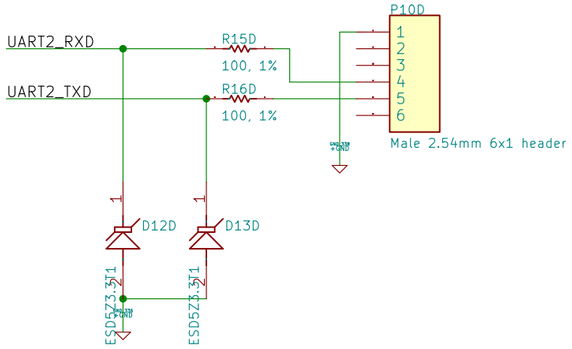
**Title: 14audio** Mamba PVT2-A

Size: B | Date: 22 12 2014 | **Rev:**
KiCad E.D.A. eeschema (2014-08-05 BZR 5054)-product | Id: 14/16

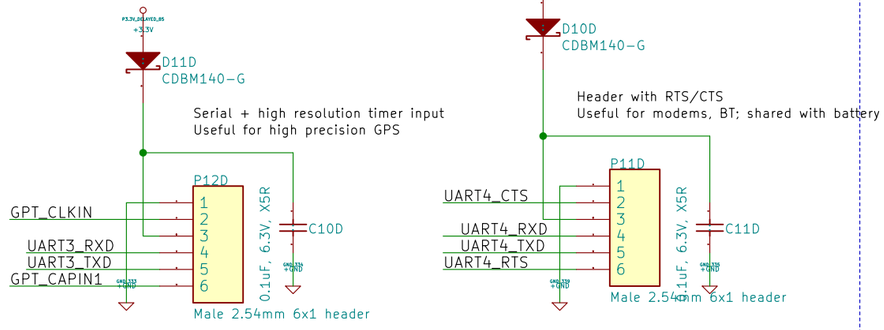

BANK 0
BANK 2
BANK 1
BANK 3
XC6SLX45-3CSG324C
default to slave serial mode
keep EIM wires as short as possible
High speed expansion notes:
All power generation is local to expansion board
Connects to 2x AD9286 or ISLA118P50 500MSPS 8-bit ADCs
8 LVDS pairs + clock in: LVDS[A,B] for OR; LVDSC for clockout
SPI CLK,DIO,CS for config (use local inverter to generate 2x CS)
19 digital I/O total ~~ 3 for SPI leaves 16 for LA use
DDC_SDA/DDC_SCL for I2C config use
Badly matched F_DX*: F_DX14, F_DX17, F_DX18 – use for SPI
Rest are matched to within 500 mil
1.23V FPGA Vcore regulator – up to 2A
1.23V enables extended MCB performance range
pin-compatible downgrade to LMR10510 / MSS5121 / CDBM140-G and half-value caps for 1A
LMR10520YSDE
2.2uH, coilcraft MSS5131-222ML
CDBMT220L-G or CDBMT240-G
Apoptosis function
SN74AUP1T97 is configured as NOR-gate, B-input inverted
When apoptosis is high, resetting the FPGA resets the CPU
Apoptosis is normally pulled down, so if unconfigured, apoptosis is effectively inactive
Setting apoptosis creates a one-way 'trap', such that the FPGA can only be configured once after boot
74AUP1T97GW
* WDOG_RST output from CPU is also provided
May be necessary to tie that to apoptosis
So a crash/watchdog reset forces apoptosis?
UIM_PWR is open-drain pulldown
MT41J128M16JT-125:K
SI4435DY
2N7002W
label pins on silk
Male 2.54mm 6x1 header
Copyright 2014 Andrew "bunnie" Huang
Novena PVT2-A
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0
Size: C,0
Date: 22 12 2014
Rev:
Id: 15/16

## Intended for external access

Console/debug UART
FTDI TTL-232R-3V3 cable pinout
Put in a convenient location

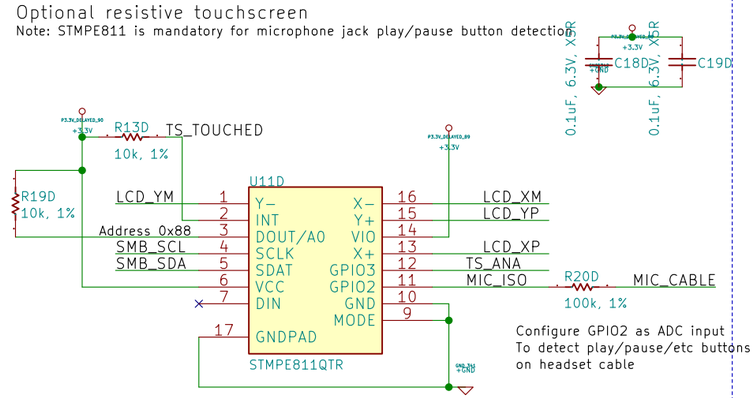



## Intended for internal module expansion




## Optional resistive touchscreen

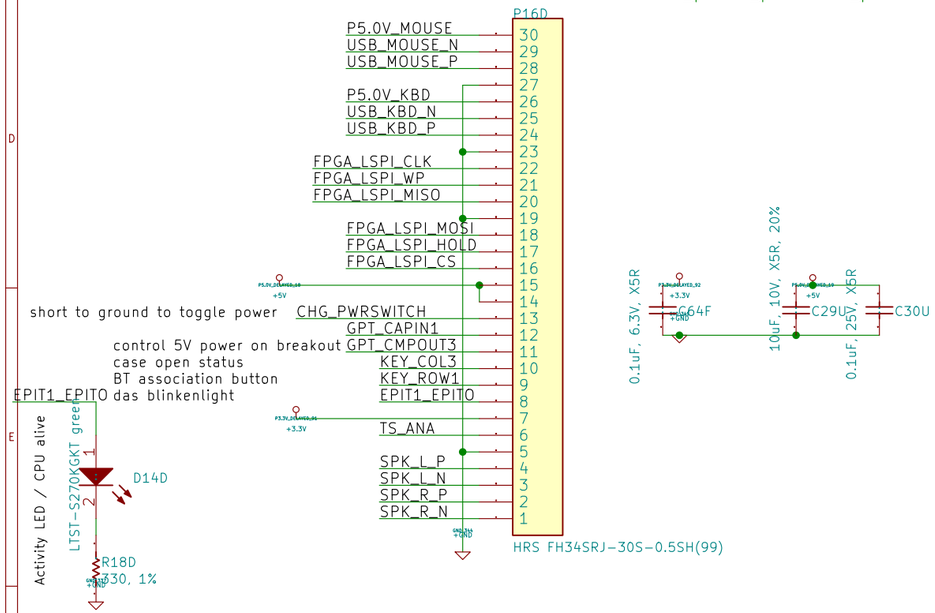
Note: STMPE811 is mandatory for microphone jack play/pause button detection

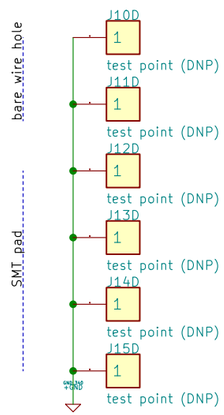


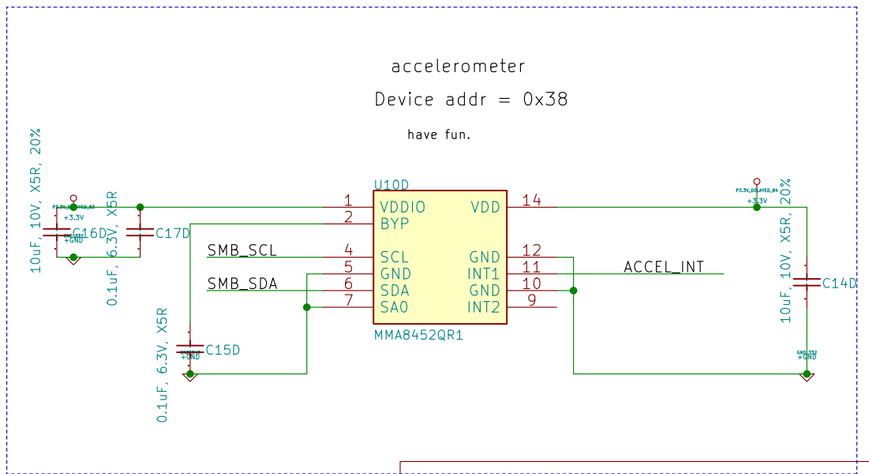

pull-ups on UART inputs to prevent spurious console events




## Front panel breakout header






Sheet: /U_16gpio_misc/
File: 16gpio_misc.sch

**Title: 16gpio_misc**

Size: B | Date: 22 12 2014 | **Rev:**
KiCad E.D.A. eeschema (2014-08-05 BZR 5054)-product | Id: 16/16