IT6251

LVDS to DispalyPort 1.1a Transmitter

Preliminary Datasheet

Specification V0.2

ITE TECH. INC.

General Description

The IT6251 is a high-performance single-chip De-SSC LVDS to DisplayPort converter. Combined with LVDS receiver and DisplayPort Transmitter, the IT6251 supports LVDS input and DisplayPort 1.1a output by conversion function. The build-in LVDS receiver can support single-link and dual-link LVDS inputs, and the build-in DisplayPort transmitter is fully compliant with DisplayPort 1.1a specification. With high speed LVDS RX, the IT6251 can support resolution up to 1080P and UXGA and 10-bit deep colors.

In order to reduce the EMI noise on legacy system application, the traditional LVDS source will transmit differential signals with spread spectrum, but this spread spectrum does not be allowed for DisplayPort protocol. The IT6251 also build-in unique De-SSC (De-Spread Spectrum) function , it can help customers easily to adopt the IT6251 on the EMI-concerned platform, with SSC has been generated from LVDS source processors.

Features (LVDS RX)

- Support LVDS Input modes: Single Link, Dual Link
- Support input clock rate up to 165MHz
- Support input color depth up to 10bit
- Support **De-SSC (De-Spread Spectrum)**
- Support Data Mapping: Open LDI / JEIDA , VESA

Features (DisplayPort TX)

- DisplayPort 1.1a transmitter
- Compliant with DisplayPort 1.1a
- Supporting two link speeds, HBR(2.7Gbps) and RBR(1.62Gbps).
- Various video input interface supporting digital video standards such as:
  - 18/24/30/36-bit RGB4:4:4
- Software programmable DispalyPort output swing and pre-emphasis level
- Embedded full-function pattern generator
- MCCS over AUX channel
- Intelligent, programmable power management

Features (Combined)

- Support up to **Full-HD/1080P** , and **WQXGA(2560x1600 RB)** display format
- Support deep color depth up to **10bit**
- 64-pin QFN (9mm x 9mm) package
- RoHS Compliant (100% Green available)

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6251	0~70	64-pin QFN	Green

Pin Diagram

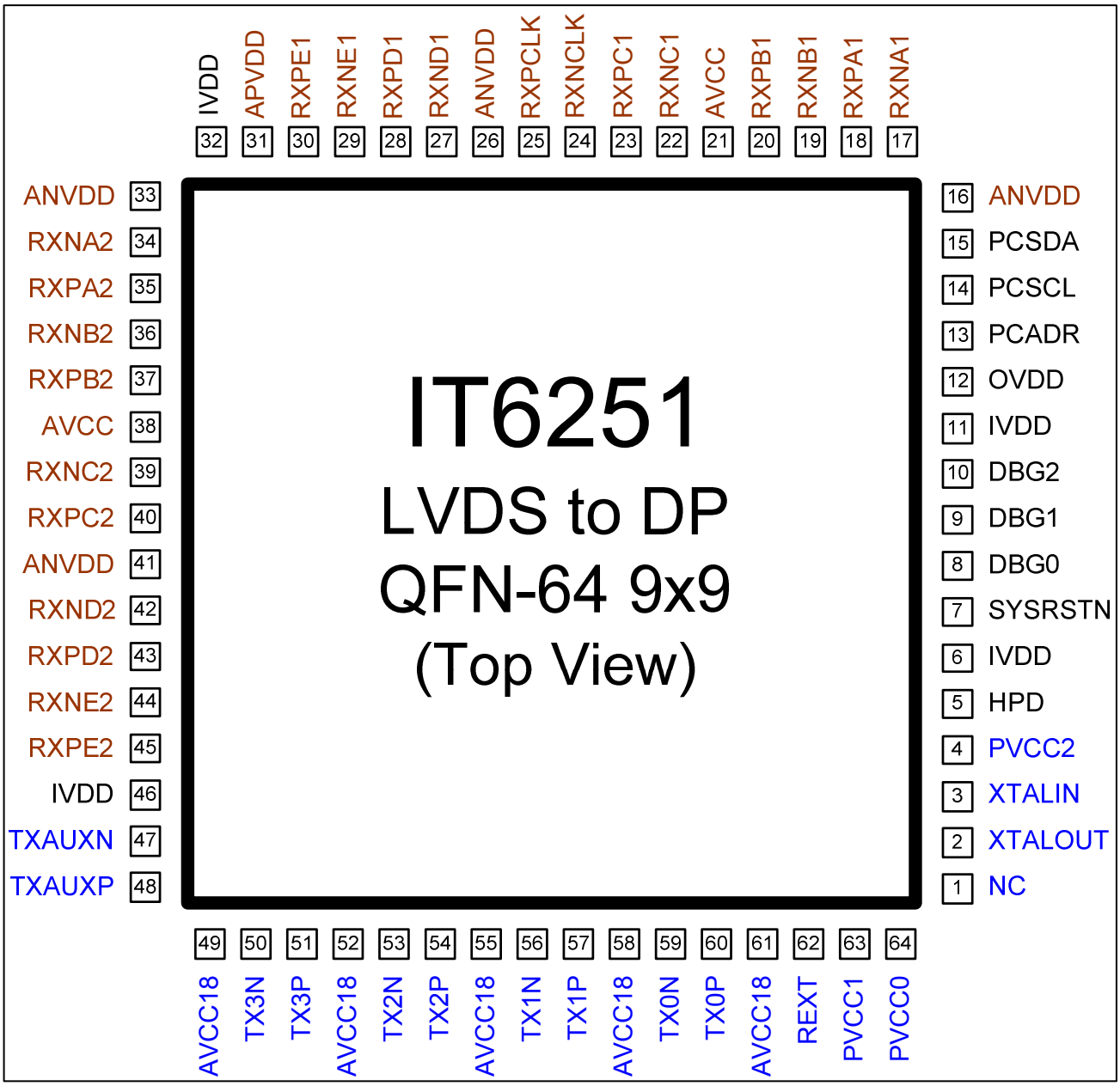


Figure 1. IT6251 pin diagram

Pin Description

LVDS front-end interface pins

Pin Name	Direction	Description	Type	Pin No.
RXNA1	Analog	LVDS first link negative input	LVDS	17
RXPA1	Analog	LVDS first link positive input	LVDS	18
RXNB1	Analog	LVDS first link negative input	LVDS	19
RXPB1	Analog	LVDS first link positive input	LVDS	20
RXNC1	Analog	LVDS first link negative input	LVDS	22
RXPC1	Analog	LVDS first link positive input	LVDS	23
RXND1	Analog	LVDS first link negative input	LVDS	27
RXPD1	Analog	LVDS first link positive input	LVDS	28
RXNE1	Analog	LVDS first link negative input	LVDS	29
RXPE1	Analog	LVDS first link positive input	LVDS	30
RXNCLK	Analog	LVDS negative clock input	LVDS	24
RXPCLK	Analog	LVDS positive clock input	LVDS	25
RXNA2	Analog	LVDS second link negative input	LVDS	34
RXPA2	Analog	LVDS second link positive input	LVDS	35
RXNB2	Analog	LVDS second link negative input	LVDS	36
RXPB2	Analog	LVDS second link positive input	LVDS	37
RXNC2	Analog	LVDS second link negative input	LVDS	39
RXPC2	Analog	LVDS second link positive input	LVDS	40
RXND2	Analog	LVDS second link negative input	LVDS	42
RXPD2	Analog	LVDS second link positive input	LVDS	43
RXNE2	Analog	LVDS second link negative input	LVDS	44
RXPE2	Analog	LVDS second link positive input	LVDS	45

Programming Pins

Pin Name	Direction	Description	Type	Pin No.
SYSRSTN	Input	Hardware reset pin. Active LOW (5V-tolerant)	LVTTL	7
PCSCL	Input	Serial Programming Clock for chip programming (5V-tolerant)	LVTTL	14
PCSDA	I/O	Serial Programming Data for chip programming (5V-tolerant)	LVTTL	15
PCADR	Input	Serial programming device address select	LVTTL	13
HPD	Input	Hot Plug Detection (5V-tolerant)	LVTTL	5

DisplayPort front-end interface pins

Pin Name	Direction	Description	Type	Pin No.
TX3P	Analog	DisplayPort Lane 3 positive output	DP	51
TX3N	Analog	DisplayPort Lane 3 negative output	DP	50
TX2P	Analog	DisplayPort Lane 2 positive output	DP	54
TX2N	Analog	DisplayPort Lane 2 negative output	DP	53
TX1P	Analog	DisplayPort Lane 1 positive output	DP	57
TX1N	Analog	DisplayPort Lane 1 negative output	DP	56
TX0P	Analog	DisplayPort Lane 0 positive output	DP	60
TX0N	Analog	DisplayPort Lane 0 negative output	DP	59
TXAUXP	Analog	DisplayPort AUX channel positive signal	DP	48
TXAUXN	Analog	DisplayPort AUX channel negative signal	DP	47
XTALIN	Analog	DisplayPort AFE crystal input (27MHz)	Analog	3
XTALOUT	Analog	DisplayPort AFE crystal output (27MHz)	Analog	2
REXT	Analog	External resistor for setting DisplayPort output level. Default tied to AVCC via a 820-Ohm SMD resistor.	Analog	62

Misc. Pins

Pin Name	Description	Type	Pin No.
DBG0	NC	LVTTL	8
DBG1	NC	LVTTL	9
DBG2	NC	LVTTL	10
NC	NC	LVTTL	1

Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD	Digital logic power (1.8V)	Power	6, 11, 32, 46
OVDD	I/O Pin power (3.3V)	Power	12
AVCC18	DisplayPort analog frontend power (1.8V)	Power	49, 52, 55, 58, 61
PVCC0	DisplayPort core PLL power (1.8V)	Power	64
PVCC1	DisplayPort core PLL power (1.8V)	Power	63
PVCC2	Filter PLL power (1.8V)	Power	4
AVCC	LVDS frontend power (3.3V)	Power	21, 38
ANVDD	LVDS frontend analog power (1.8V)	Power	16, 26, 33, 41
APVDD	LVDS frontend PLL power (1.8V)	Ground	31
GND	Exposed GND pad	Ground	65

Functional Description

Block Diagram

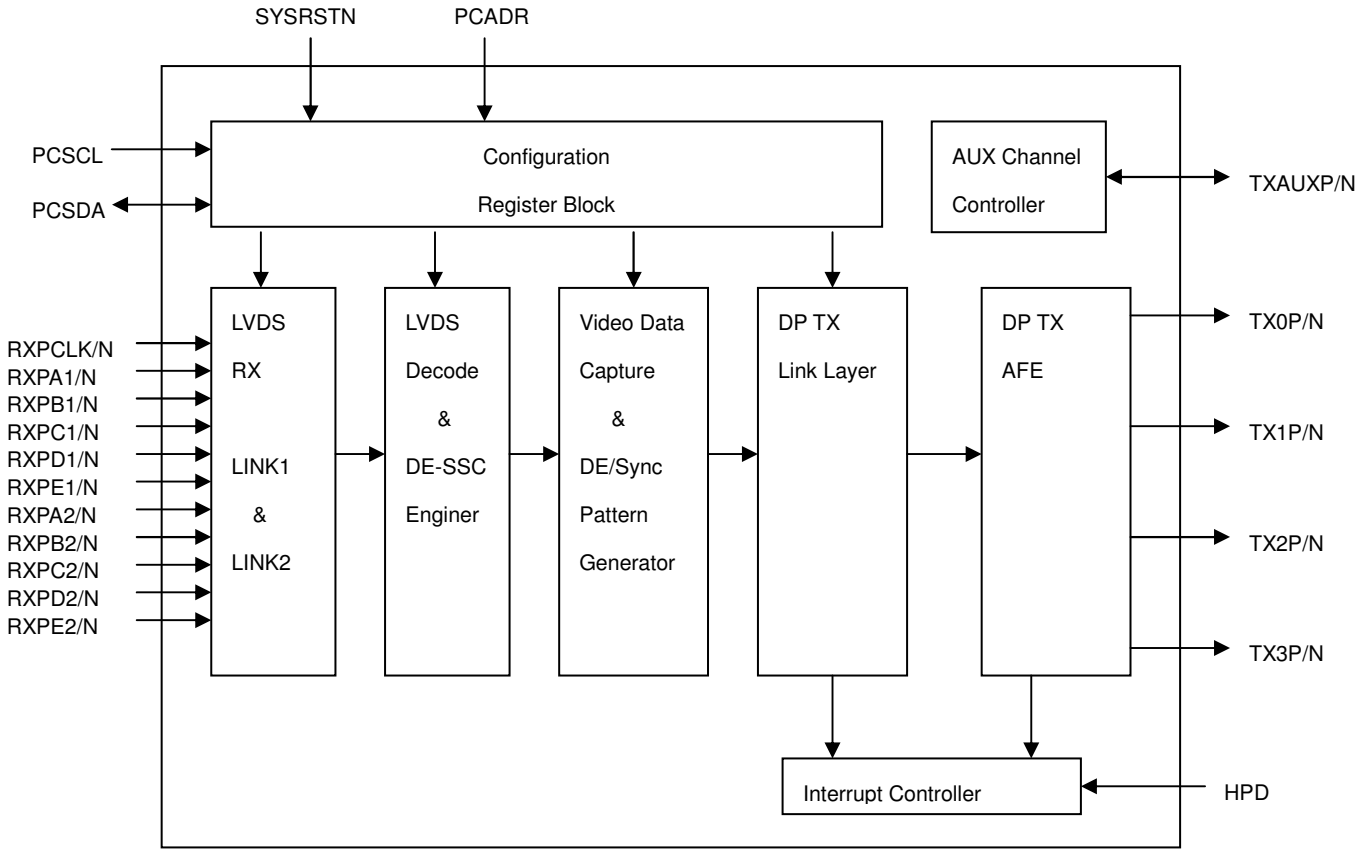
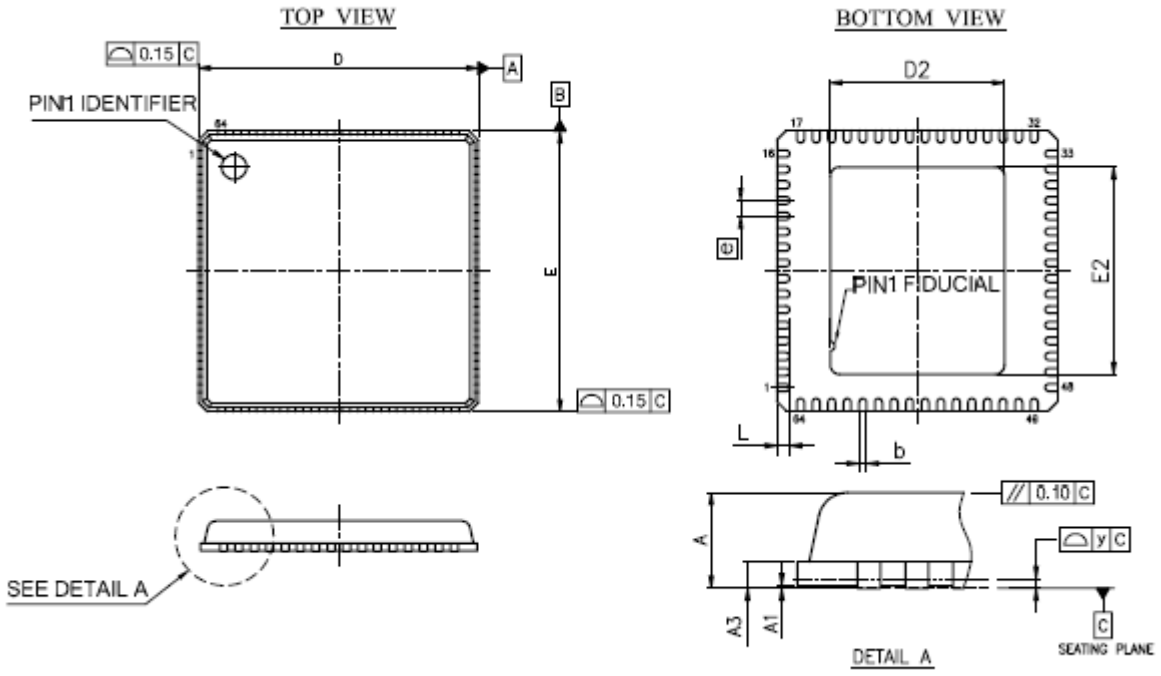


Figure 2. Functional block diagram of IT6251

Package Dimensions



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.031	0.035	0.039	0.80	0.90	1.00
A1	0.000	0.001	0.002	0.00	0.02	0.05
A3	0.008 REF			0.20 REF		
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.350	0.354	0.358	8.90	9.00	9.10
D2	0.141	0.149	0.157	3.58	3.78	3.98
E	0.350	0.354	0.358	8.90	9.00	9.10
E2	0.141	0.149	0.157	3.58	3.78	3.98
e	0.020 BSC			0.50 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50
y	--	--	0.003	--	--	0.08

Figure 3. 64-pin QFN Package Dimensions