First International Computer,Inc

Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : XY680

Version : 0.1

Initial Date : 11. 28 , 2007

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3. Block Diagram :
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5. Board Stack up Description :
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9. switch setting

Manager Sign by: AVERY

Drawing by : Jack & Victor

Total confirm by: AVERY

LAN Circuit check by:

Audio Circuit check by:

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5FL.,NO.300,Yang Guang St.,Neihu
114 TAIPEI, TAIWAN,ROC
(886-2)8751-8751

Title: XY680>Penryn+Candiga GM45+ICH9M

Size: C | Document Number: Title | Rev: 0.2

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1. Schematic Page Description :

XY670 Schematic Ver : 0.1

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34. NB9P-GS MIOA/B/GPIO
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37. NEW CARD (EXPRESS CARD)
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39. PCIE LAN PHY 82567LF
40.TRANSFORMER
41. E-SATA/MB_USB/EXT_USB_TV
42. SATA HDD/ODD CON
43. FW322(IEEE1394)
44. AZALIA ALC888S-VC-GR
45. SP/HP AMP APA2068KAI
46. Audio CON/MIC/WOFER
47. Cardreader RTS5168
48. K/B /GP/DIP/RF-WLAN
49. CCD/Bluetooth/MMB/LED
50. PMX
51. POWER BLOCK
52. ACIN,BATIN,DCIN
53. Charge
54. 3/5VDDA/S/M,1.5VDDA
55. DRAM POWER/1.5VDDS/M,0.75VDDS
56.1.5VDDM Cantiga VGA power
57. VGA Core Power
58. 1.8VDDM,1.2VDDM
59. CPU Core Power*
60. Daughter board Audio JACK
61. Daughter board Battery/Power/Wlan LED
62. Daughter board PWR/SW
63. Daughter board Mini-TV/USB port
64. Daughter board external ODD for 18"
65. Daughter board Glide pad for 18"

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	FW322 (IEEE1394)
AD27	X
AD29	X

BUSMASTER

REQ	CHIP
REQ0 / GNT0	X
REQ1 / GNT1	FW322
REQ2 / GNT2	X
REQ3 / GNT3	X
REQ4 / GNT4	X

IRQ Channel	Desciption
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Casacde)
IRQ3	LAN / MODEM
IRQ4	~~Serial Port~~
IRQ5	AUDIO / VGA / USB
IRQ6	~~FLOPPY DISK~~
IRQ7	~~LPT~~
IRQ8	RTC
IRQ9	ACPI
IRQ10	FIR (Disable by default) (MODEM/LAN)
IRQ11	~~Cardbus~~
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

DMA Channel	Device
DMA0	FIR (disable by default) (MODEM / LAN)
DMA1	
DMA2	
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

PCIINT	CHIP
IRQA	IEEE1394 (FW322)
IRQB	
IRQC	X
IRQD	X
IRQE / GPIO2	
IRQE / GPIO3	X
IRQE / GPIO4	PASS0
IRQE / GPIO5	CRISIS

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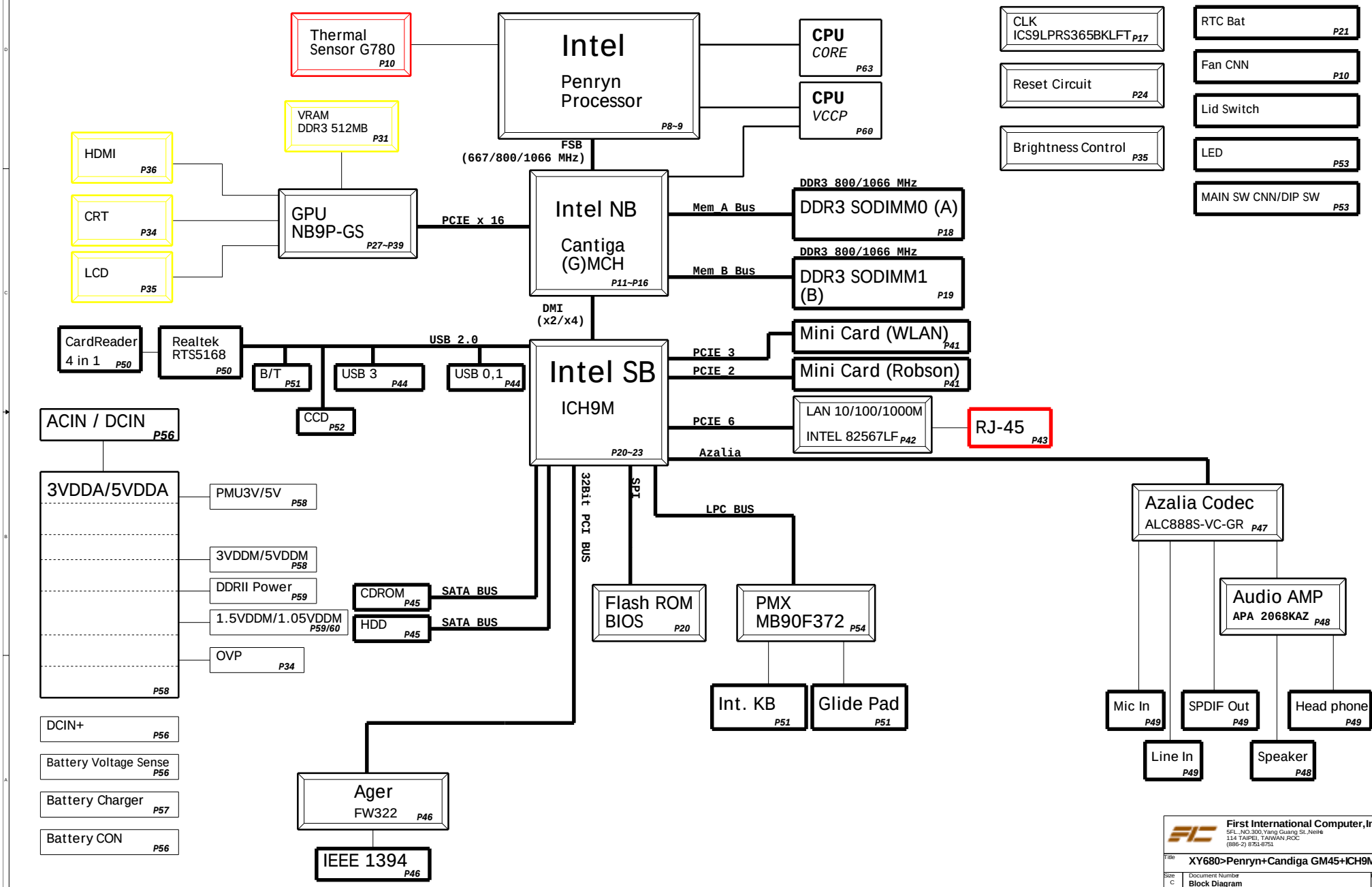
3. Block Diagram :



4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON
3VDDA	3.3V always on power rail by DCON
3VDDS	3.3V power rail by PSUSC#
5VDDS	5.0V power rail by PSUSC#
3VDDM	3.3V switched power rail by SUSTAT_B#
5VDDM	5.0V switched power rail by SUSTAT_B#
VCC_CORE	Core Voltage for CPU
1.05VDDM	1.05V power rail for AGTL+ termination/Core for GMCH by SUSTAT_B#
1.5VDDM	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH7m by SUSTAT_B#
1.8VDDS	1.8V power rail for DDRII by PSUSC#
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SUSTAT_B#

Part Naming Conventions

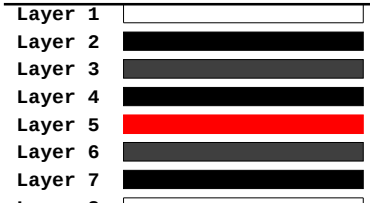
C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

= Active Low signal

5. Board Stack up Description

PCB Layers



Layer 1 Component Side, Microstrip signal Layer
Layer 2 Ground Plane
Layer 3 Stripline Layer(High Speed)
Layer 4 Normal Signal / Ground 1 Plane
Layer 5 Power Plane
Layer 6 Stripline Layer(High Speed)
Layer 7 Ground 2 Plane
Layer 8 Solder Side,Microstrip signal Layer

Layers : 8 Depth 1.2mm Impence 55 ohms +/- 10%

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

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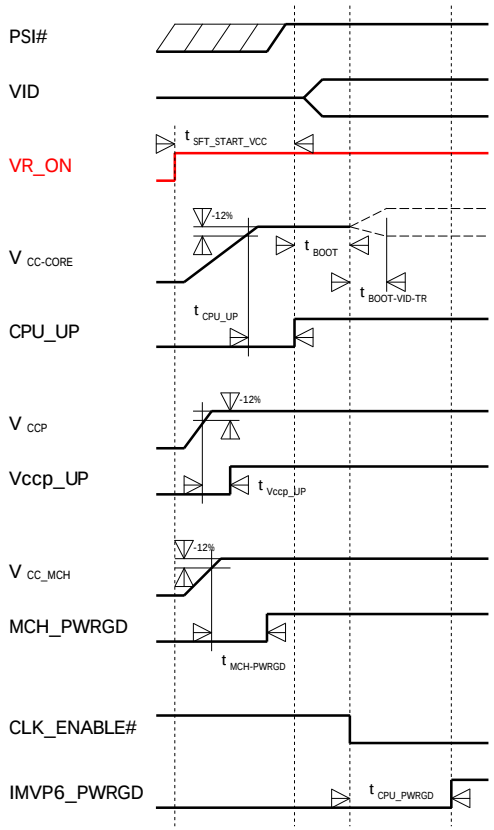
7. power on & off & S3 Sequence :

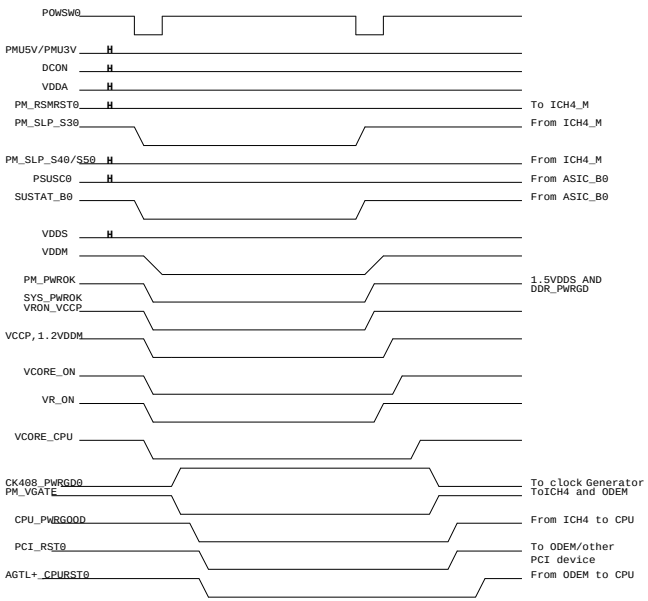
Power On Sequencing Timing Diag ram

20060117A - DATA FROM NO.16809

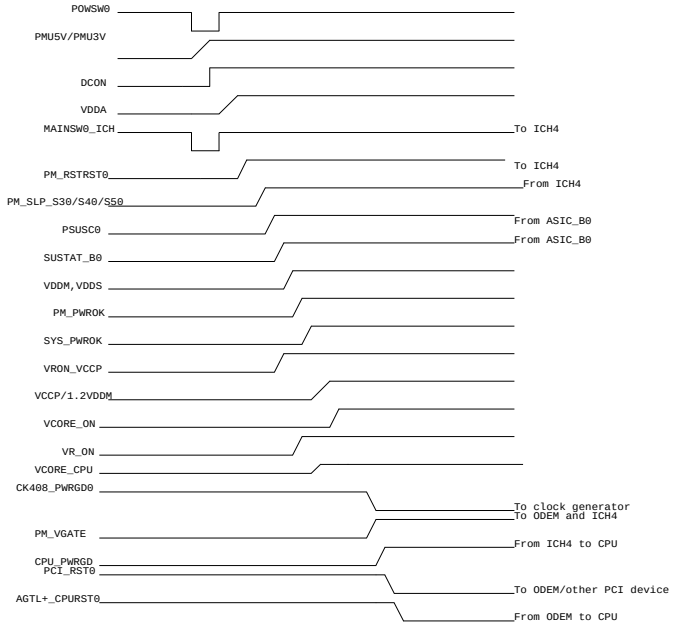


$t_{SFT\_START\_VCC}$	Max = 3 ms
t_{BOOT}	Min = 10 us , Max = 100 us
$t_{BOOT-VID-TR}$	Max = 100 us
t_{CPU_UP}	Min = 10 us , Max = 30 us
t_{Vccp_UP}	Min = 10 us , Max = 30 us
$t_{MCH-PWRGD}$	Min = 10 us , Max = 30 us
t_{CPU_PWRGD}	Min = 3 ms , Max = 20 ms

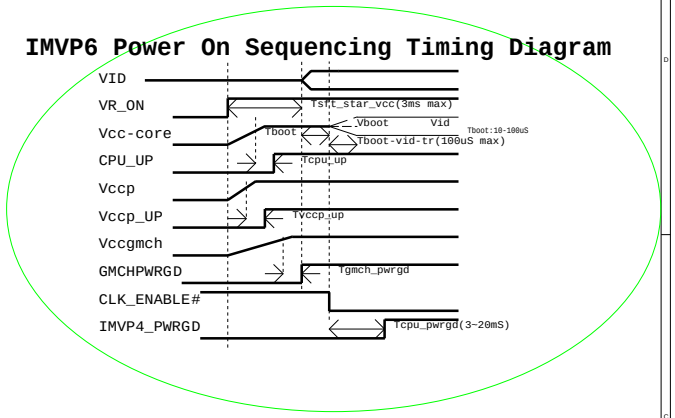
S3 SUSPEND AND RESUME TIMING



BATTERY ONLY POWER ON TIMING



IMVP6 Power On Sequencing Timing Diagram



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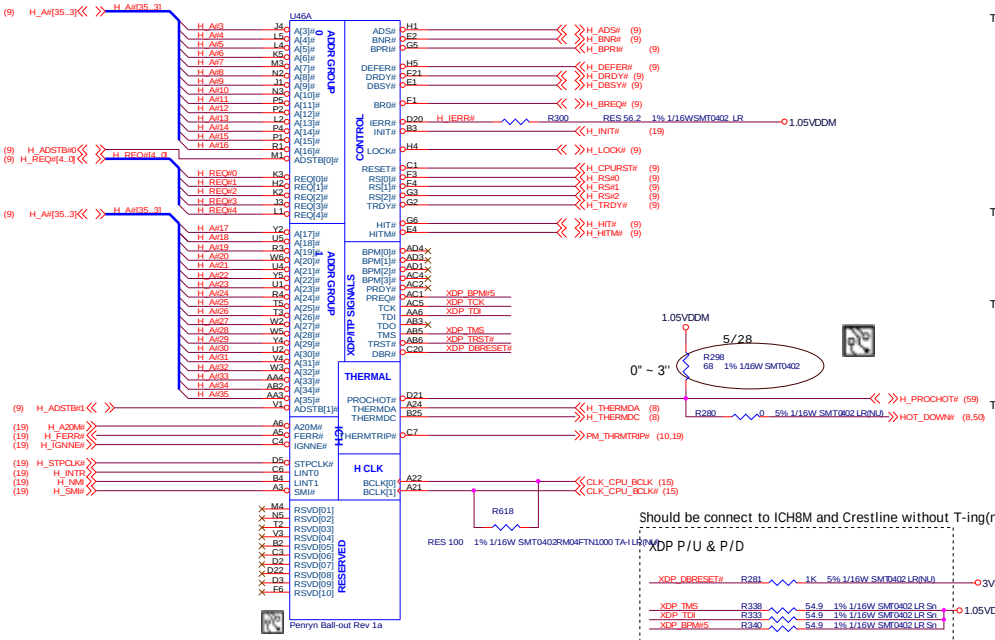
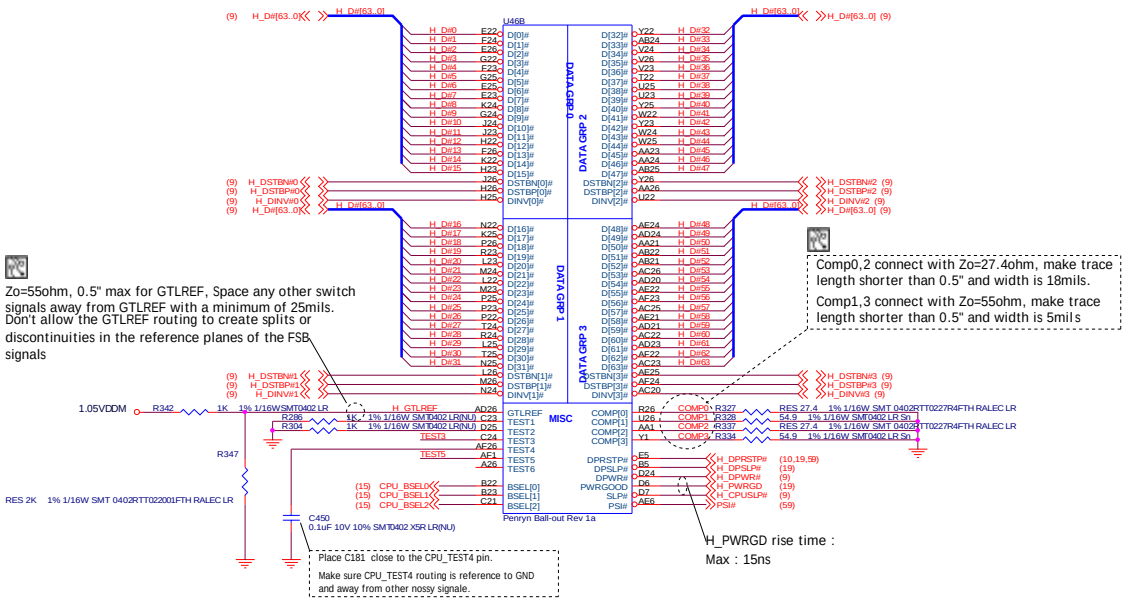
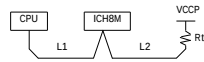


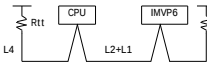


VCCP=1.05VDDM

Topology : FERR#

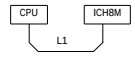


L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	56 +/-5%	Microstrip
0.5" - 12"	0" - 3.0"	56 +/-5%	Stripline



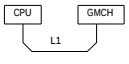
L1	L2	L3	L4	Rtt	Transmission Line
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	75 +/-5%	Micro-strip
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	75 +/-5%	Strip-line

Topology : PWRGOOD



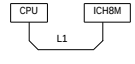
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : CPUSLP#



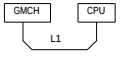
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : INTR , NMI , A20M# , DPSLP# , IGNNE# , INIT# , SMI# , STPCLK#



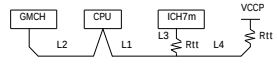
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : RESET#



L1	Transmission Line
1" - 6"	Micro-strip
1" - 6"	Strip-line

Topology : THERMTRIP#



L1	L2	L1+L3	L3	L4	Rss	Rtt	Transmission Line
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Micro-strip
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Strip-line

Processor ITP Signal Default Strapping When ITP-XDP & ITP700FLEX Dedbug Port Not Used.

Signal	Resistor Value	Connect To	Resistor Placement
TDI	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TMS	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TRST#	649 OHM +/-5%	GND	Within 2.0" of the CPU
TCK	54.9 OHM +/-5%	GND	Within 2.0" of the CPU
TDO	OPEN	NC	N/A

FSB Common Clock Signal Layout Guide :

ADS# , BNR# , BPRI# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# , HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#.			
Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 ~ 6.5 inch	55+/-15%	4 & 8 mils
Micro-strip(Ext. Layer)			5 & 10 mils

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
DATA#[15..0] , DINV0#	+/- 100 mils	DSTBP0#,DSTBN0#	+/- 25 mils
DATA#[31..16] , DINV1#	+/- 100 mils	DSTBP1#,DSTBN1#	+/- 25 mils
DATA#[47..32] , DINV2#	+/- 100 mils	DSTBP2#,DSTBN2#	+/- 25 mils
DATA#[63..48] , DINV3#	+/- 100 mils	DSTBP3#,DSTBN3#	+/- 25 mils

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)	
				Data-to-Data,Strobe-to-strobe	Strobe-to-Data
DINV#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DATA#[63..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DSTBN#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils
DSTBP#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils

FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
A#[16..3] , REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 200 mils
A#[31..17]	+/- 200 mils	ADSTB1#	+/- 200 mils

*** No length matching requirements exist between ADSTB0# and ADSTB1#

FSB Source Synchronous Address Signal Routing :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
Address#[31..3]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
REQ#[4..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
ADSTB#[1..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils

(7,9,10,12,13,15,19,21,56) 1.05VDDM — 1.05VDDM

(8,10,13,15,16,17,18,19,20,21,22,30,31,32,33,37,38,43,44,46,48,49,54,55,56,57,59) 3VDDM — 3VDDM

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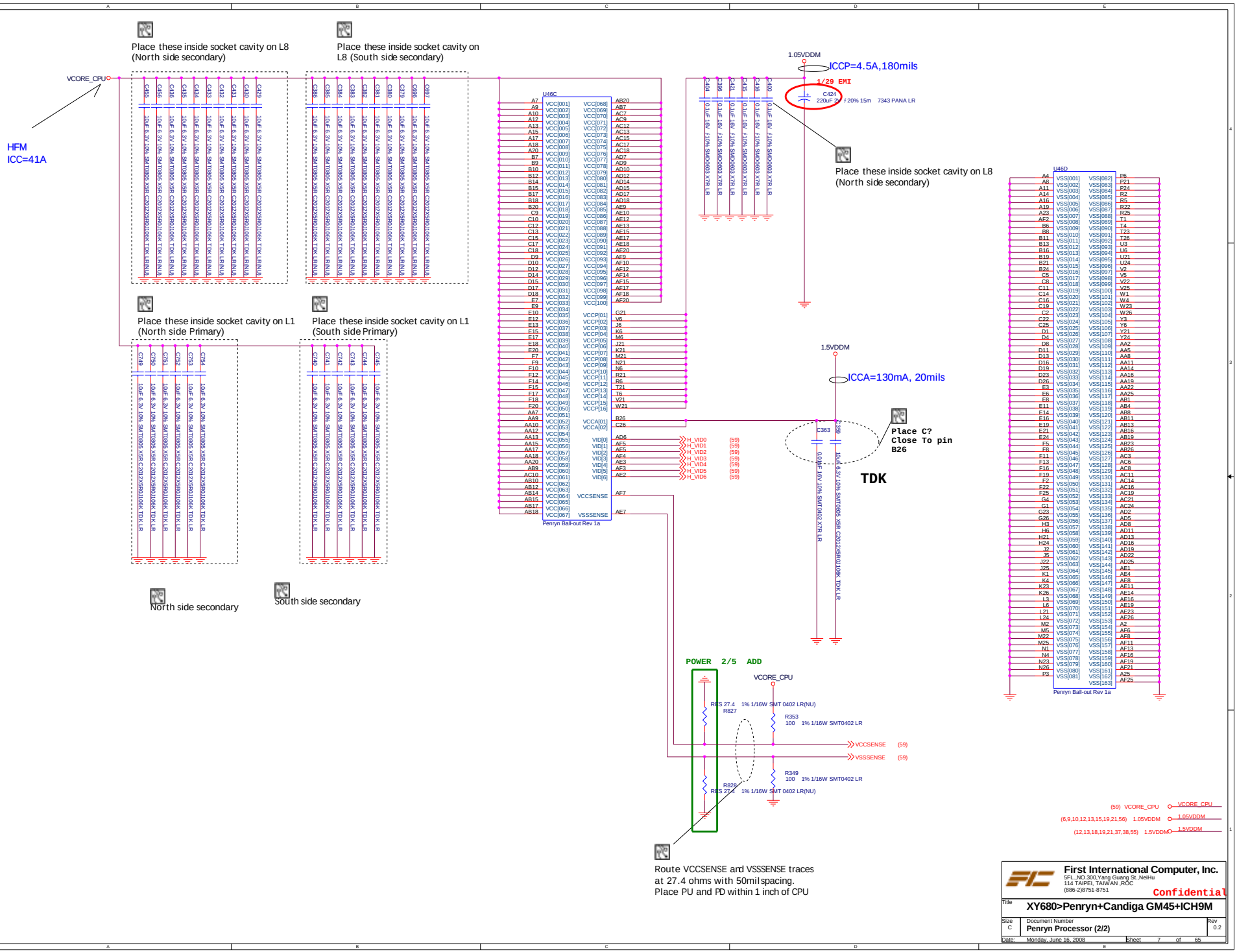
Place these inside socket cavity on L8
(North side secondary)
Place these inside socket cavity on
L8 (South side secondary)
VCORE_CPU
HFM
ICC=41A
1.05VDDM
ICCP=4.5A,180mils
1/29 EMI
C424
220uF 2V / 20% 15m 7343 PANA LR
Place these inside socket cavity on L8
(North side secondary)
Place these inside socket cavity on L1
(North side Primary)
Place these inside socket cavity on L1
(South side Primary)
1.5VDDM
ICCA=130mA, 20mils
Place C?
Close To pin
B26
TDK
POWER 2/5 ADD
VCORE_CPU
R827
R353
100 1% 1/16W SMT0402 LR
R828
R349
100 1% 1/16W SMT0402 LR
VCCSENSE (59)
VSSSENSE (59)
North side secondary
South side secondary
Route VCCSENSE and VSSSENSE traces
at 27.4 ohms with 50mil spacing.
Place PU and PD within 1 inch of CPU
(59) VCORE_CPU
(6,9,10,12,13,15,19,21,56) 1.05VDDM
(12,13,18,19,21,37,38,55) 1.5VDDM
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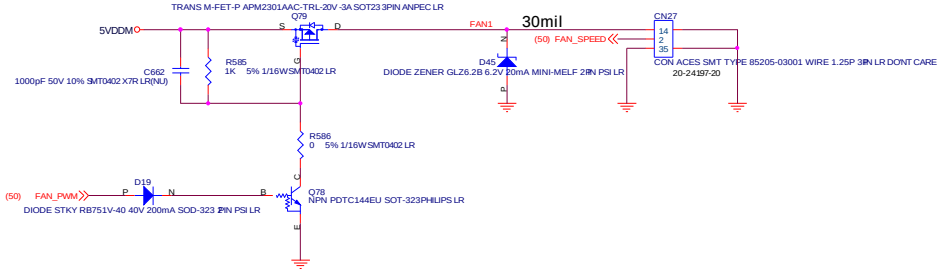
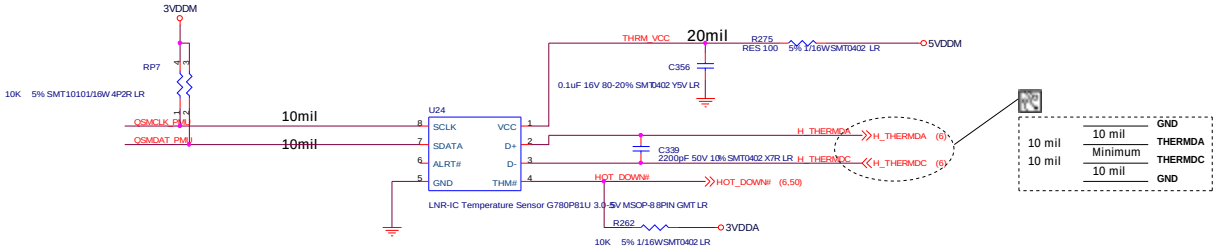
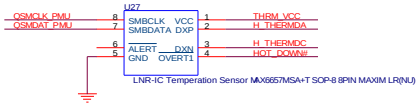
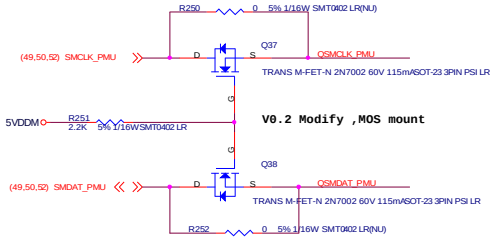


CPU Termal Sensor



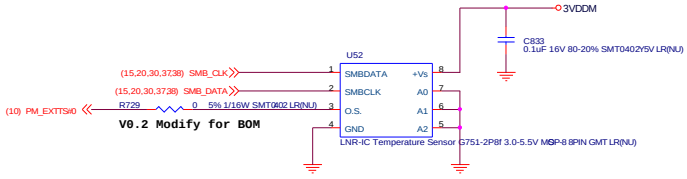
Reserve for Material shortage





DDR THERMAL SENSOR

CLOSE TO DDR DIMM



(6,10,13,15,16,17,18,19,20,21,22,30,31,32,33,37,38,43,44,46,48,49,54,55,56,57,59) 3VDDM
(18,20,21,22,24,32,37,38,39,41,45,47,48,49,50,54,55,58) 3VDDA
(16,20,21,30,31,33,42,44,45,46,48,54,56,57,59) 5VDDM

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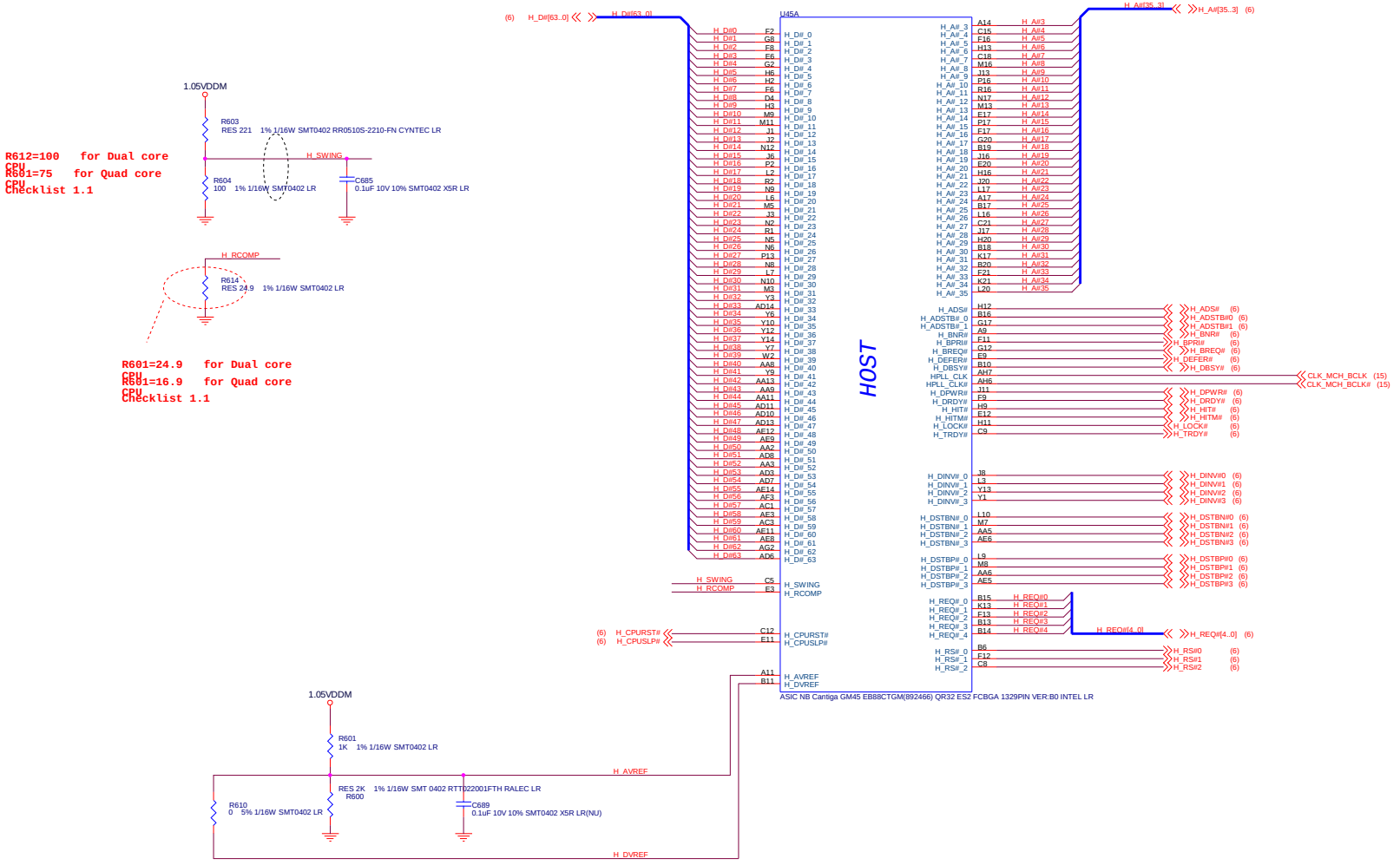
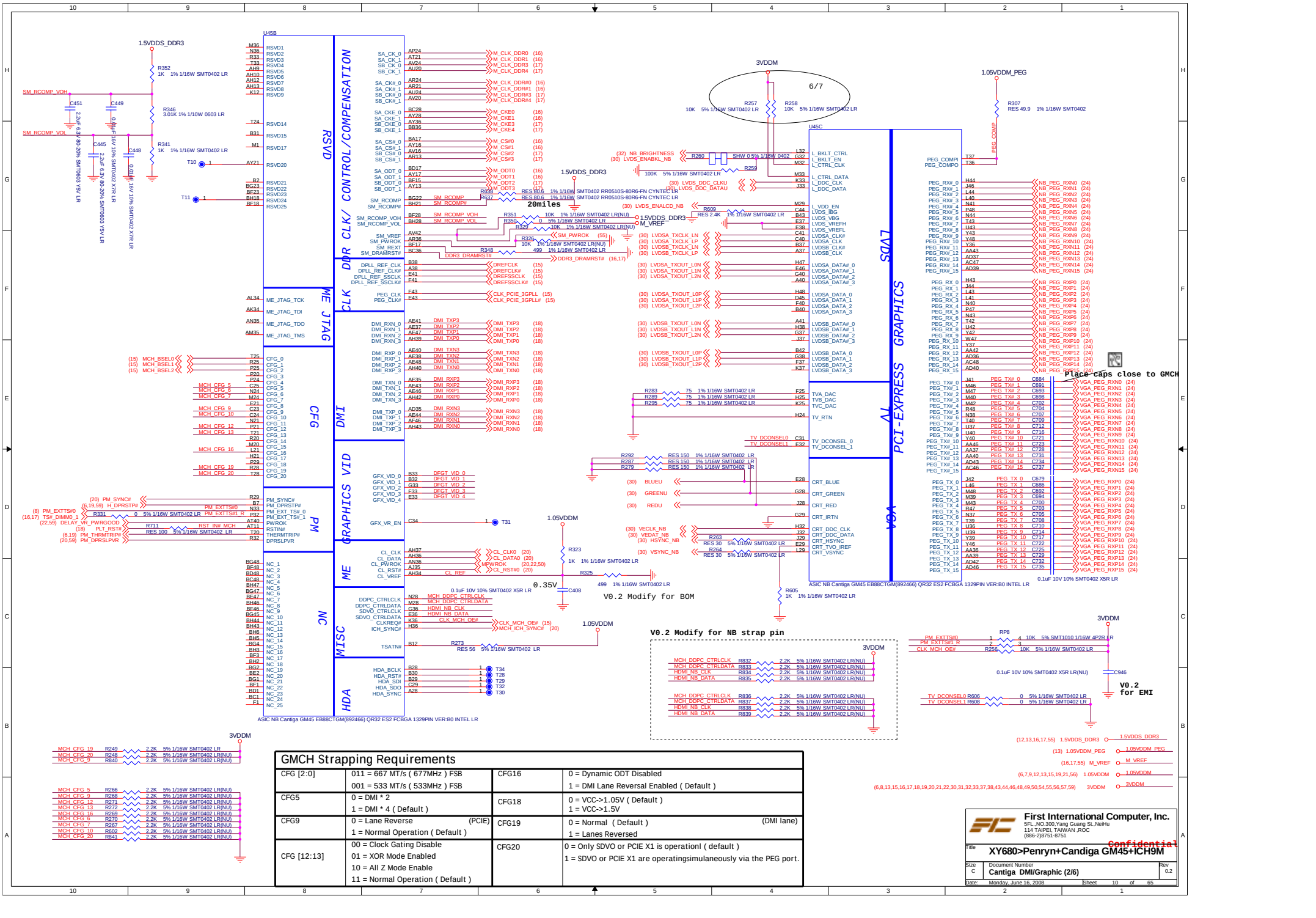
NB Cantiga 88CTGMB-OES

BOM is 05-23881-02



(6,7,10,12,13,15,19,21,56) 1.05VDDM 1.05VDDM

First International Computer, Inc. 5FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)8751-8751	Confidential	
Title: XY680>Penryn+Candiga GM45+ICH9M		
Size: C	Document Number: Cantiga Host (1/6)	Rev: 0.2
Date: Monday, June 16, 2008	Sheet 9 of 65	



GMCH Strapping Requirements

CFG [2:0]	011 = 667 MT/s (677MHz) FSB 001 = 533 MT/s (533MHz) FSB	CFG16	0 = Dynamic ODT Disabled 1 = DMI Lane Reversal Enabled (Default)
CFG5	0 = DMI * 2 1 = DMI * 4 (Default)	CFG18	0 = VCC->1.05V (Default) 1 = VCC->1.5V
CFG9	0 = Lane Reverse (PCIE) 1 = Normal Operation (Default)	CFG19	0 = Normal (Default) (DMI lane) 1 = Lanes Reversed
CFG [12:13]	00 = Clock Gating Disable 01 = XOR Mode Enabled 10 = All Z Mode Enable 11 = Normal Operation (Default)	CFG20	0 = Only SDVO or PCIE X1 is operationl (default) 1 = SDVO or PCIE X1 are operatingsimulaneously via the PEG port.

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Title: XY680>Penryn+Candiga GM45+ICH9M

Size	Document Number	Rev
C	Cantiga DMI/Graphic (2/6)	0.2

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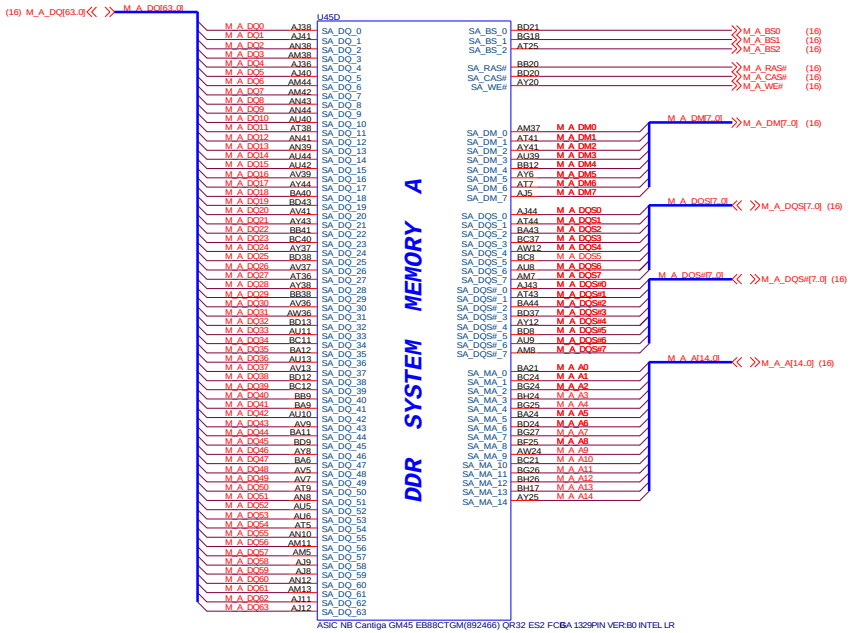
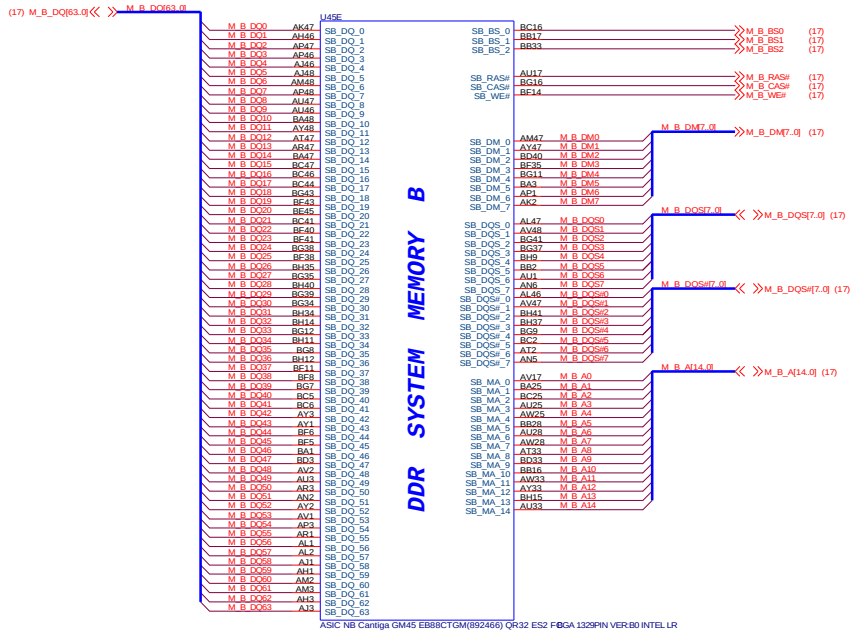
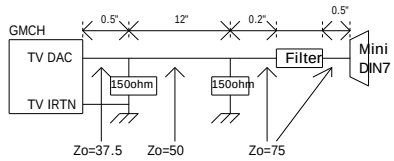




TV DAC Routing Guideline

1. The minimum spacing between each RGB is 40-mils while 50-mils is preferred
2. RGB signals should be routed on the same layer, have a similar number of bends, same number of vias
3. All routing should be done with ground referencing as well
4. TV DAC route lengths should be lenght match to within 200 mils



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Title: XY680>Penryn+Candiga GM45+ICH9M

Size: C | Document Number: Cantiga DDR2 (3/6) | Rev: 0.2

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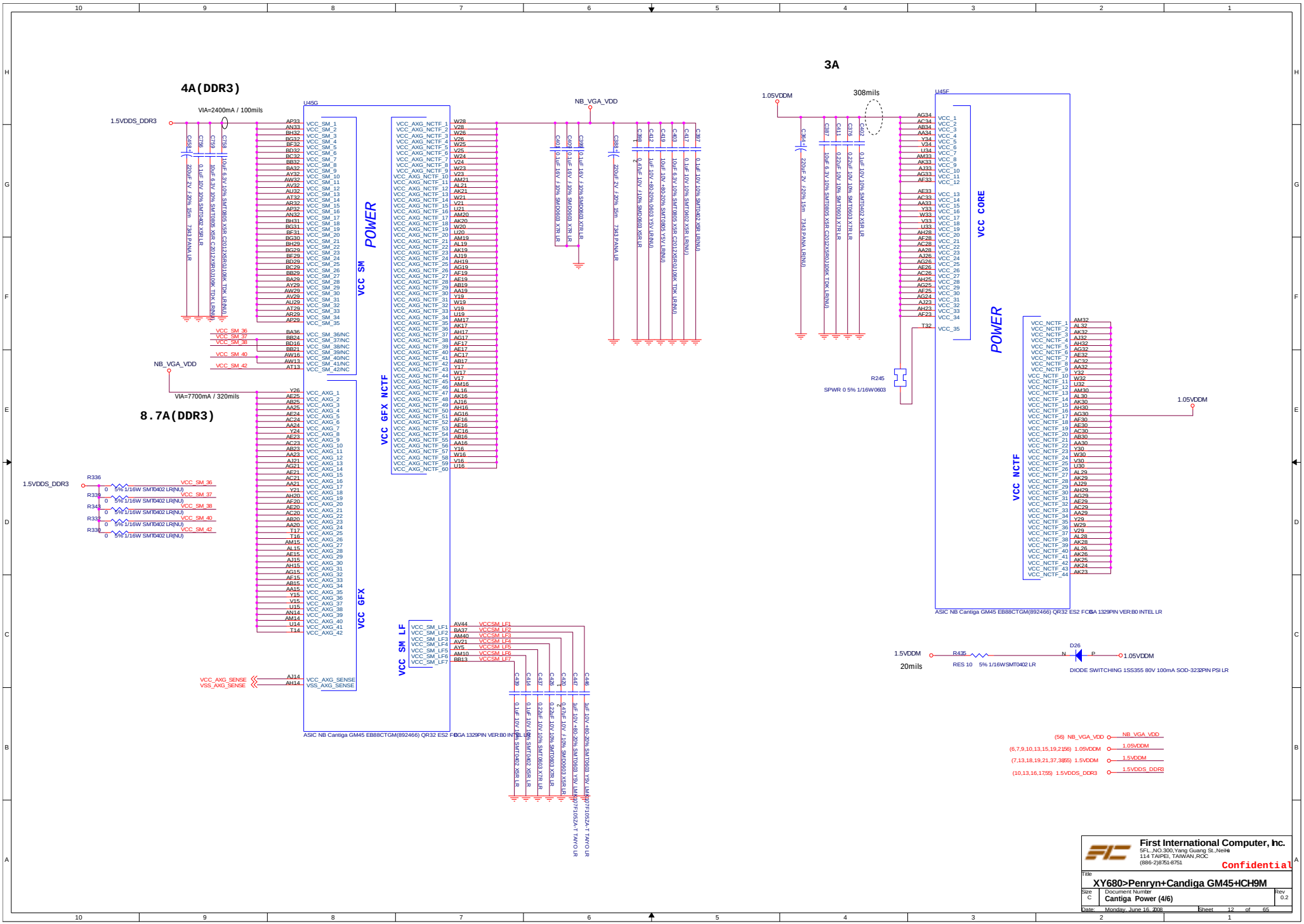
4A(DDR3)
8.7A(DDR3)
3A
VCC SM POWER
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC CORE POWER
VCC NCTF
1.5VDDS_DDR3
NB_VGA_VDD
1.05VDDM
VIA=2400mA / 100mils
VIA=7700mA / 320mils
308mils
20mils
ASIC NB Cantiga GM45 EB88CTGM(892466) QR32 ES2 FCBGA 1329PIN VER:B0 INTEL LR
SPWR 0 5% 1/16W 0603
RES 10 5% 1/16W SMT0402 LR
DIODE SWITCHING 1SS355 80V 100mA SOD-323 2PIN PSI LR
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XY680>Penryn+Candiga GM45+ICH9M
Cantiga Power (4/6)
Monday, June 16, 2008
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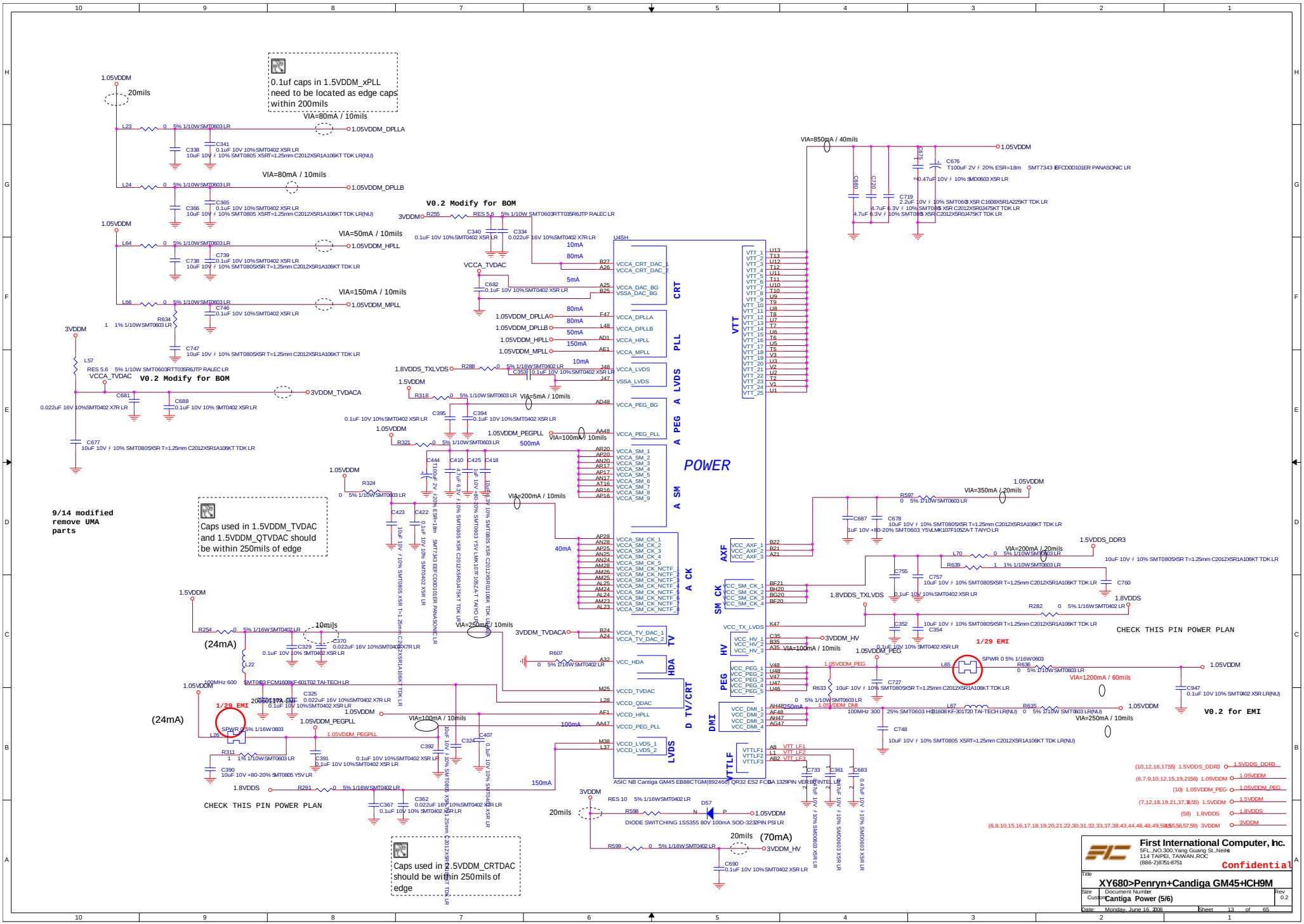
0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils
V0.2 Modify for BOM
POWER
9/14 modified remove UMA parts
Caps used in 1.5VDDM_TVDAC and 1.5VDDM_QTVDAC should be within 250mils of edge
Caps used in 2.5VDDM_CRTDAC should be within 250mils of edge
CHECK THIS PIN POWER PLAN
CHECK THIS PIN POWER PLAN
1/29 EMI
V0.2 for EMI
ASIC NB Cantiga GM45 EB88CTGM(892466) QR32 ES2 FCBA 1329PIN VERSION INTEL
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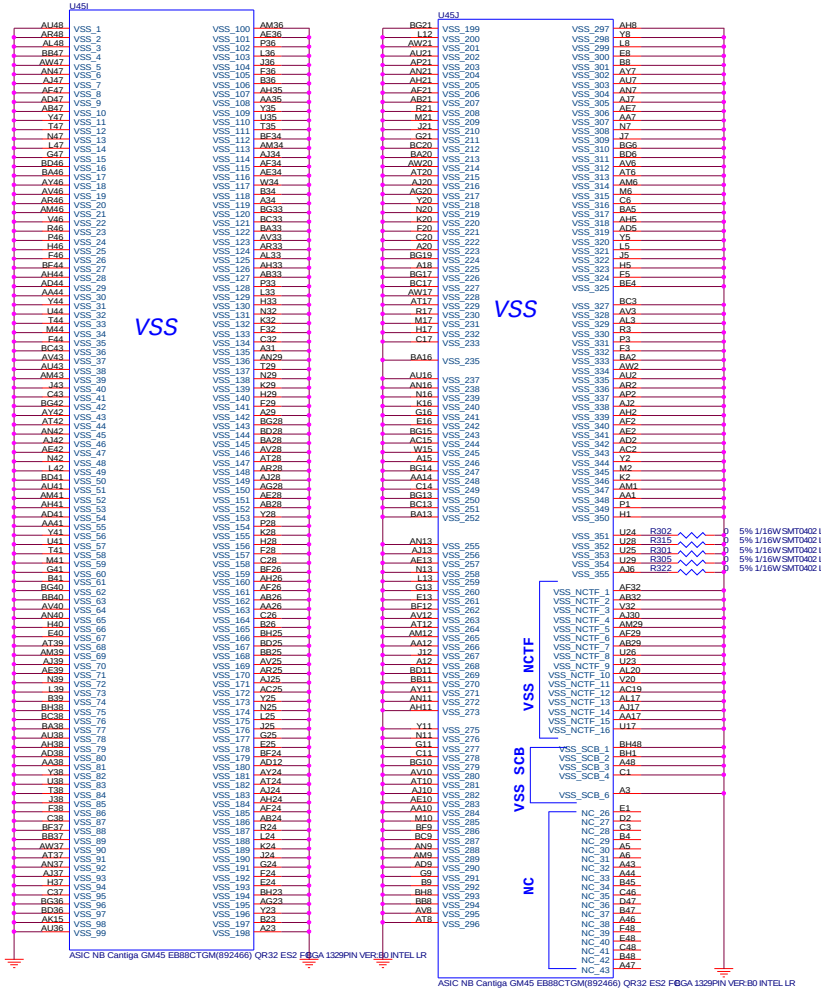
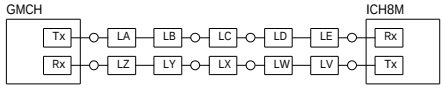
XY680>Penryn+Cantiga GM45+ICH9M
Cantiga Power (5/6)
Rev 0.2
Monday, June 16, 2008
Sheet 13 of 65



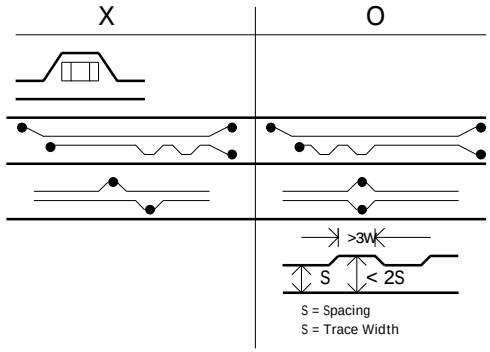
DMI Routing Guideline



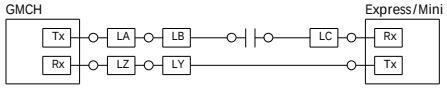
Breakout/in LA/LZ	Main Route LB/LY	Main Route LD/LW	Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Dididerential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane spli ts No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 400 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+L C+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differenti al pair to +/- 5 mils



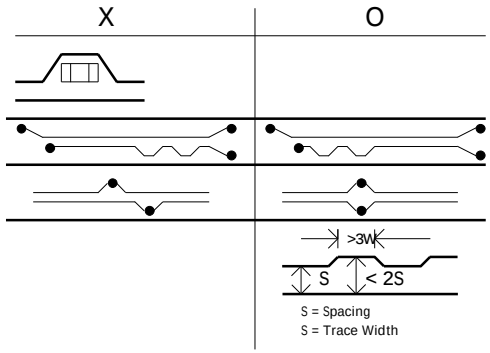
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane spli ts No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differenti al pair to +/- 5 mils



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Title: XY680>Penryn+Candiga GM45+ICH9M

Size: C | Document Number: Cantiga Ground (6/6) | Rev: 0.2

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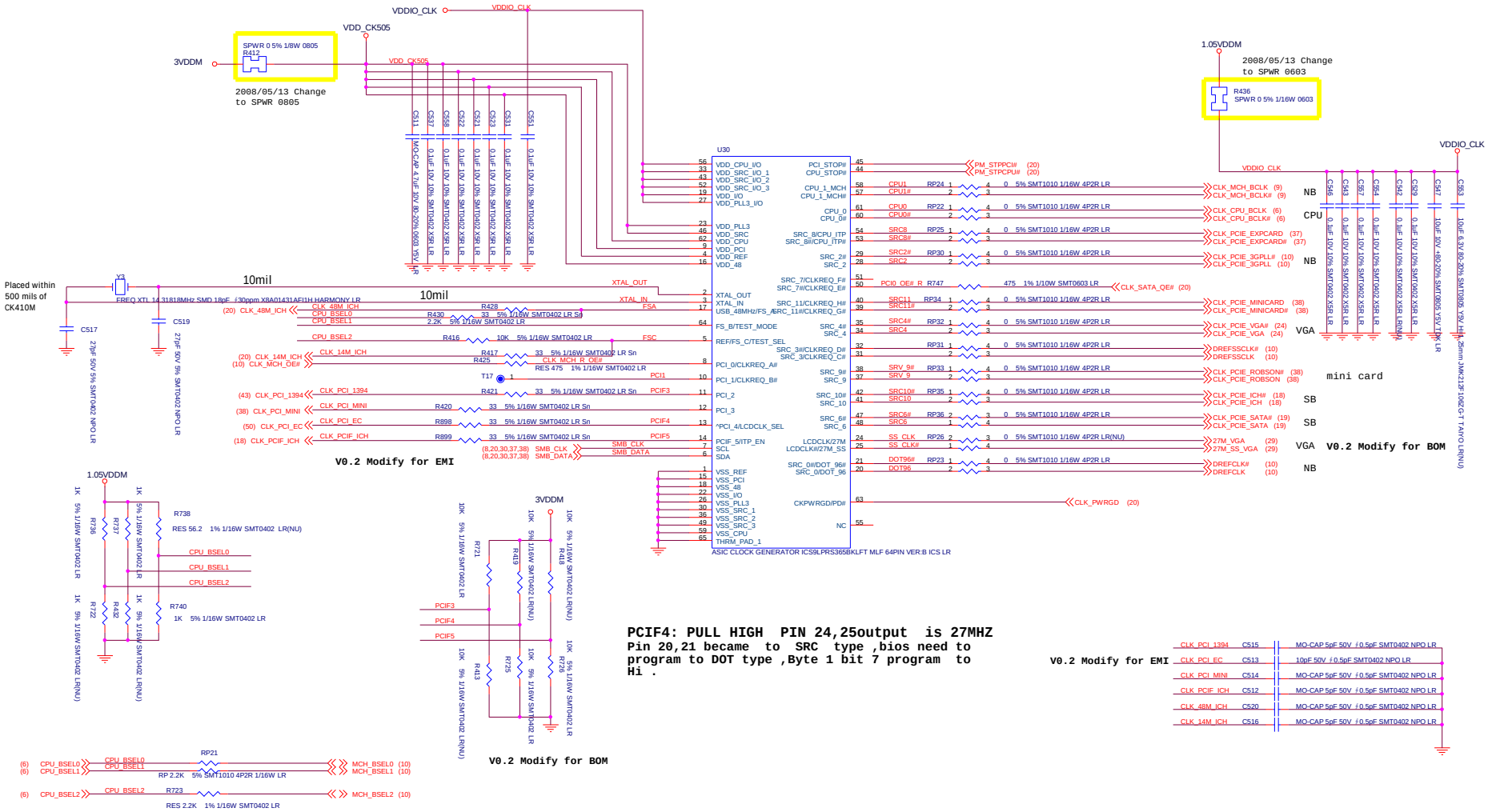

FSC	FSB	FSA	Host Clock
CPU_BSEL2	CPU_BSEL1	CPU_BSEL0	Frequency MHz
0	1	1	166
0	1	0	200

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
0	0	0	0	DOWN	0.8
0	0	0	1	DOWN	1.0
0	0	1	0	DOWN	1.25
0	0	1	1	DOWN	1.5
0	1	0	0	DOWN	1.75
0	1	0	1	DOWN	2.0
0	1	1	0	DOWN	2.5
0	1	1	1	DOWN	3.0

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
1	0	0	0	Center	+/- 0.3
1	0	0	1	Center	+/- 0.4
1	0	1	0	Center	+/- 0.5
1	0	1	1	Center	+/- 0.6
1	1	0	0	Center	+/- 0.8
1	1	0	1	Center	+/- 1.0
1	1	1	0	Center	+/- 1.25
1	1	1	1	Center	+/- 1.5

(6,7,9,10,12,13,19,21,56) 1.05VDDM
(6,8,10,13,16,17,18,19,20,21,22,30,31,32,33,37,38,43,44,46,48,49,50,54,55,56,57,59) 3VDDM
(8,18,20,21,22,24,32,37,38,39,41,45,47,48,49,50,52,54,55,58) 3VDDA

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Title: XY680>Penryn+Candiga GM45+ICH9M

Size: C | Document Number: Clock Generator IC ICS9LP505-1 | Rev: 0.2

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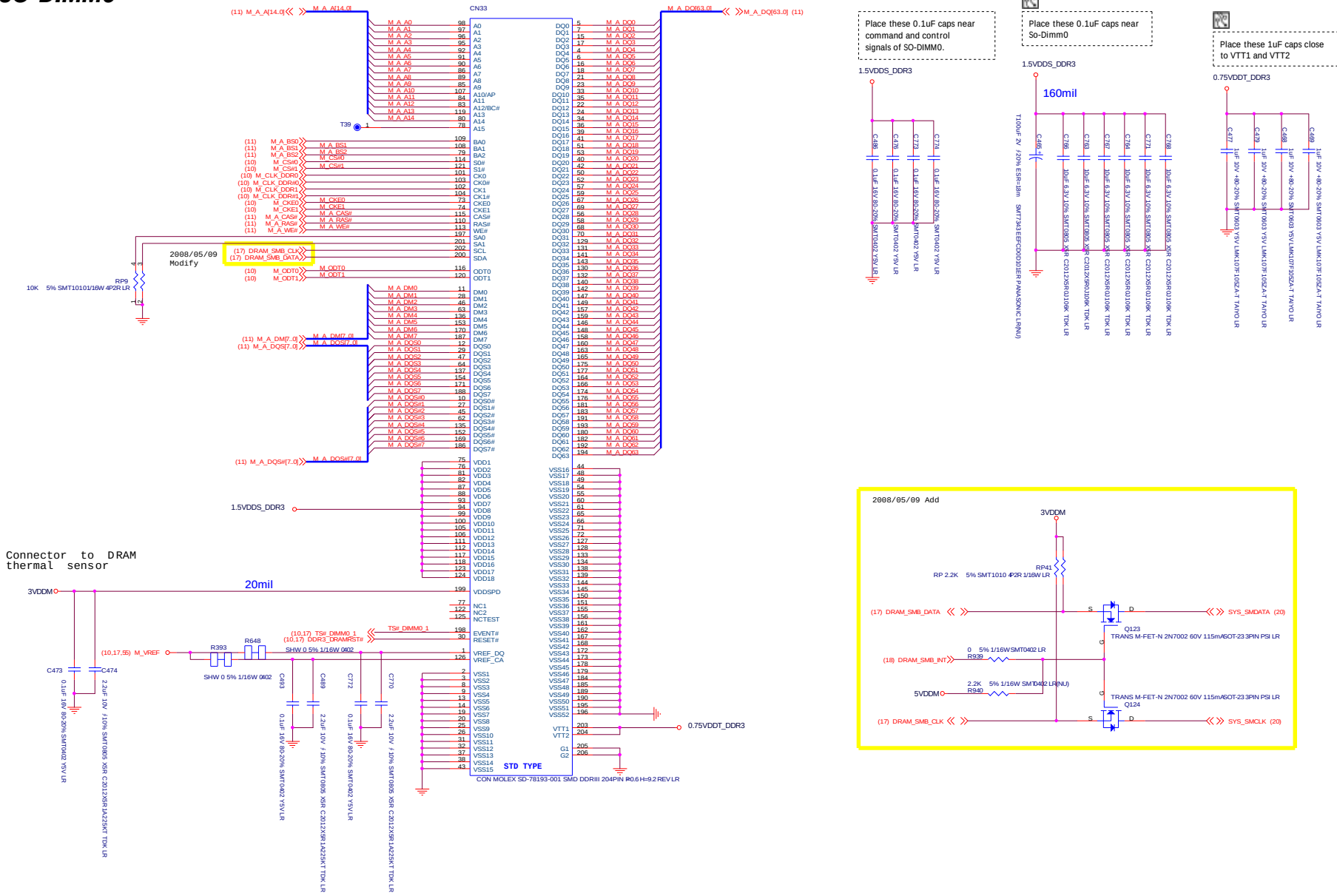
SO-DIMM0



Place these 0.1uF caps near command and control signals of SO-DIMM0.

Place these 0.1uF caps near So-Dimm0

Place these 1uF caps close to VTT1 and VTT2

2008/05/09 Add

(8,20,21,30,31,33,42,44,45,46,48,54,56,57,59) 5VDDM
(10,17,55) M_VREF
(17,55) 0.75VDDT_DDR3
(10,12,13,17,55) 1.5VDDS_DDR3
(6,8,10,13,15,17,18,19,20,21,22,30,31,32,33,37,38,43,44,46,48,49,50,55,56,57,59) 3VDDM
(8,18,20,21,22,24,32,37,38,39,41,45,47,48,49,50,52,54,55,58) 3VDDA

5VDDM	5VDDM
M_VREF	M_VREF
0.75VDDT_DDR3	0.75VDDT_DDR3
1.5VDDS_DDR3	1.5VDDS_DDR3
3VDDM	3VDDM
3VDDA	3VDDA

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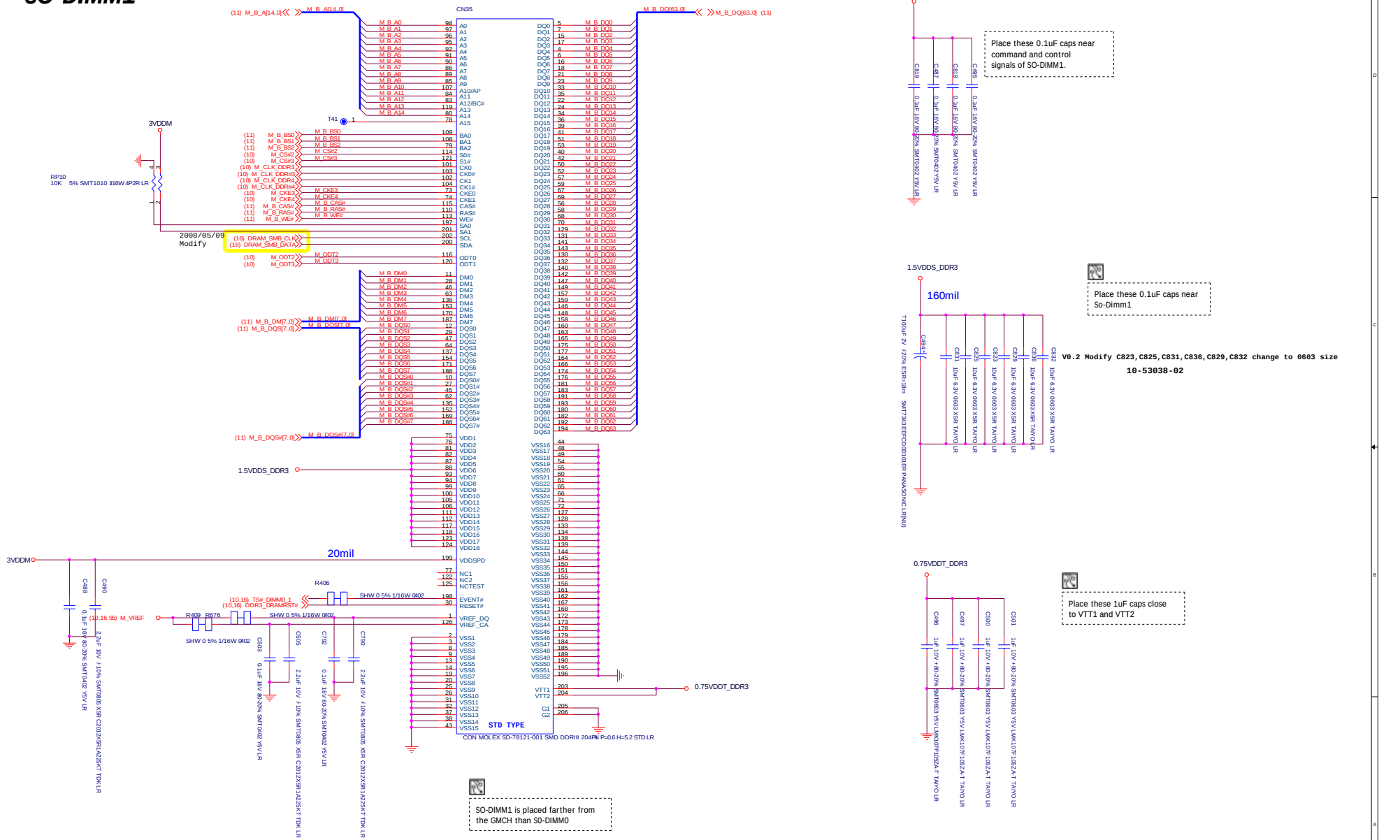
Title	XY680>Penryn+Candiga GM45+ICH9M	
Size C	Document Number DDR3 SDRAM SO-DIMM0	Rev 0.2
Date: Monday, June 16, 2008	Sheet 16 of 65	

SO-DIMM1



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Title	XY680>Penryn+Candiga GM45+ICH9M
Size C	Document Number DDR3 SDRAM SO-DIMM1
Rev	0.2
Date: Monday, June 16, 2008	Sheet 17 of 65

ICH9 82801IBM A-2
ICH9 82801IEM A-2 ENHANCED

PCIE AC coupling caps need to be within 250mils of the driver

BOM is 05-23900-01 ENHANCE

EXPRESS CARD

MINI CARD (WIRELESS)

MINI CARD (Robson)

LAN

PCI-Express Media Interface

USB

SPI

3VDDM

R734 2.2K 5% 1/16W SMT0402 LR

R731 2.2K 5% 1/16W SMT0402 LR

Q98

(43) PCI_PME#

PCI_Q_PME#

TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR

1.5VDDM

R761 RES 24.9 1% 1/16W SMT0402 LR

Place within 500mils of ICH

- M/B USB PORT
- E-SATA USB PORT
- EXT USB PORT
- Express Card
- TV_Tuner
- EXT USB PORT
- MINI CARD (WIRELESS)
- CCD
- CARD READER
- MINI CARD (Roboson)
- BLUE TOOTH
- USB_RF_Bluetooth

2008/05/07 Re-arrange port

V0.2 Modify

2008/05/09 Modify

R842 10K 5% 1/16W SMT0402 LR OC3#

R843 10K 5% 1/16W SMT0402 LR HYBRID_RST#

RP28 10K 5% SMT2010 1/16W 8P4R LR

RP20 10K 5% SMT1010 1/16W 4P2R LR

RP29 10K 5% SMT2010 1/16W 8P4R LR

DRAM_SMB_INT

DRAM_SMB_INT (16)

3VDDA

TV_ON

HYBRID_RST#

OC11#

USB_RBIAS_PN

R449 RES 20 1% 1/16W SMT0402 LR

2008/04/21 Change R449 from 22.6 to 20 .

Place within 500mils of ICH 5/5 mils spacing on microstrip

ASIC SB ICH9M NH82801IBM(888758) QP23 ES2 mBGA 676PIN VER:A2 INTEL LR

PCI Pull up

RP16 8.2K 5% SMT2010 1/16W 8P4R LR

RP12 8.2K 5% SMT2010 1/16W 8P4R LR

RP13 8.2K 5% SMT2010 1/16W 8P4R LR

RP18 8.2K 5% SMT2010 1/16W 8P4R LR

RP15 8.2K 5% SMT2010 1/16W 8P4R LR

RP14 8.2K 5% SMT2010 1/16W 8P4R LR

PCI

Interrupt I/F

1394

HYBRID POWER

CRT_DDC_SW (30)

HYBRID VGA RSEST

R237 10K 5% 1/16W SMT0402 LR(NU)

R724 1K 5% 1/16W SMT0402 LR

R844 10K 5% 1/16W SMT0402 LR(NU)

R864 10K 5% 1/16W SMT0402 LR(NU)

R730 1K 5% 1/16W SMT0402 LR(NU)

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override Strap	
PCI_GNT#3	Low = A16 swap override enabled High = Default

SPI Interface

C797 0.1uF 16V 80-20% SMT0402 Y5V LR

10 mils

U49

R670 3.3K 5% 1/16W SMT0402 LR

R671 3.3K 5% 1/16W SMT0402 LR

FLASHROM Serial Flash SPI W25X80VSSI 8Mbit 2.7V~3.6V SOIC(208mil) 8PIN WINBOND LR

U49 V0.2 Modify for BOM change to 16M

3VDDM

C816 0.1uF 16V 80-20% SMT0402 Y5V LR

U51

PLT_RST#

SB/LAN/CD-ROM/EXPRESS CARD/Mini Card

BUF_PLT_RST# (24,37,38,47,50)

DL-IC NC7S08P5X_NL SC70 5PIN FAIRCHILD LR

Buffer to reduce loading on PLT_RST#

R715 100K 5% 1/16W SMT0402 LR

(7,12,13,19,21,37,38,55) 1.5VDDM

(6,8,10,13,15,16,17,19,20,21,22,30,31,32,33,37,38,43,44,46,48,49,50,54,55,56,57,59) 3VDDM

(8,20,21,22,24,32,37,38,39,41,45,47,48,49,50,54,55,58) 3VDDA

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Title: XY680>Penryn+Candiga GM45+ICH9M

Size: C | Document Number: ICH9M PCI/PCIE/DMI (1/4) | Rev: 0.2

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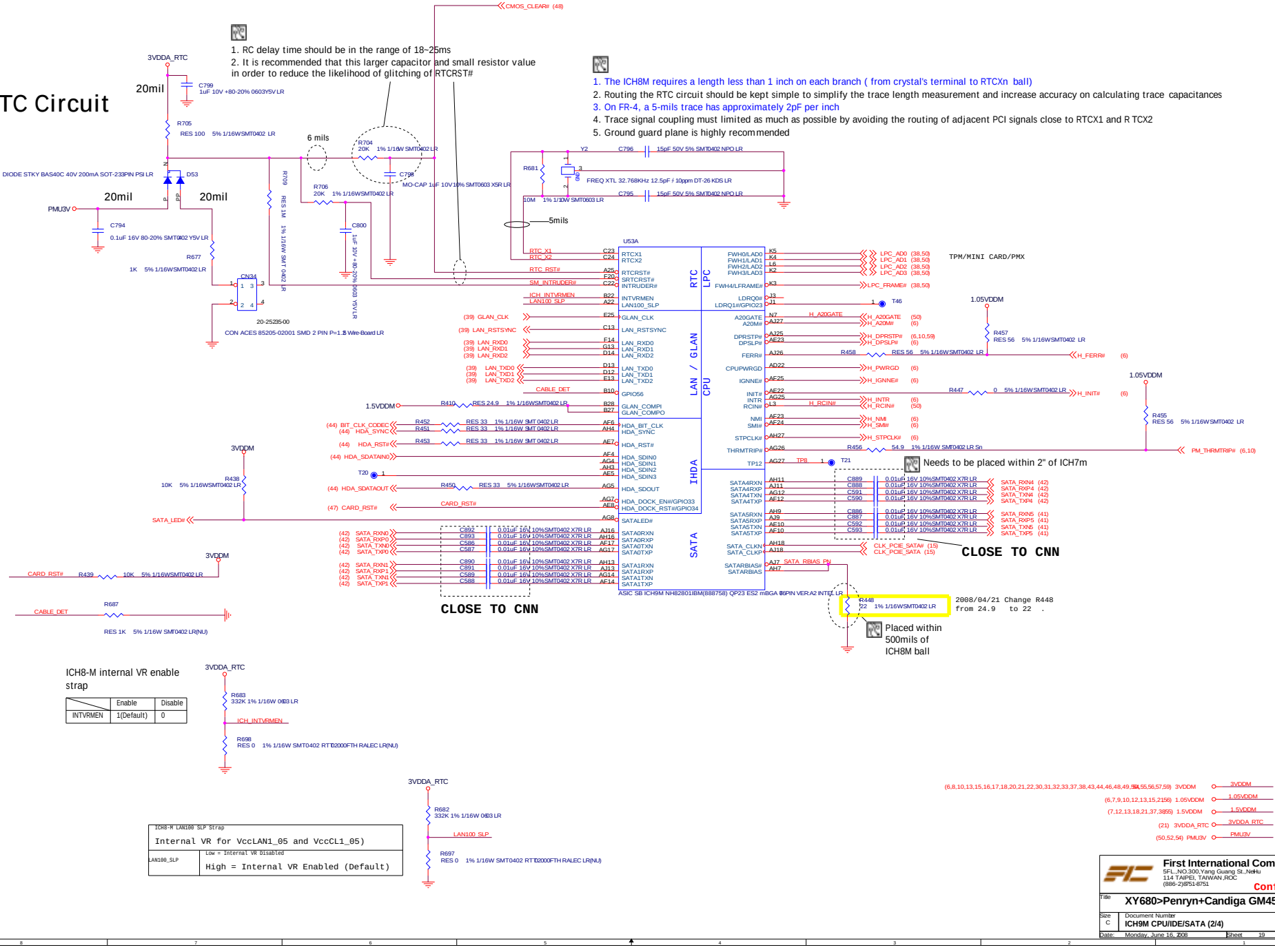
RTC Circuit



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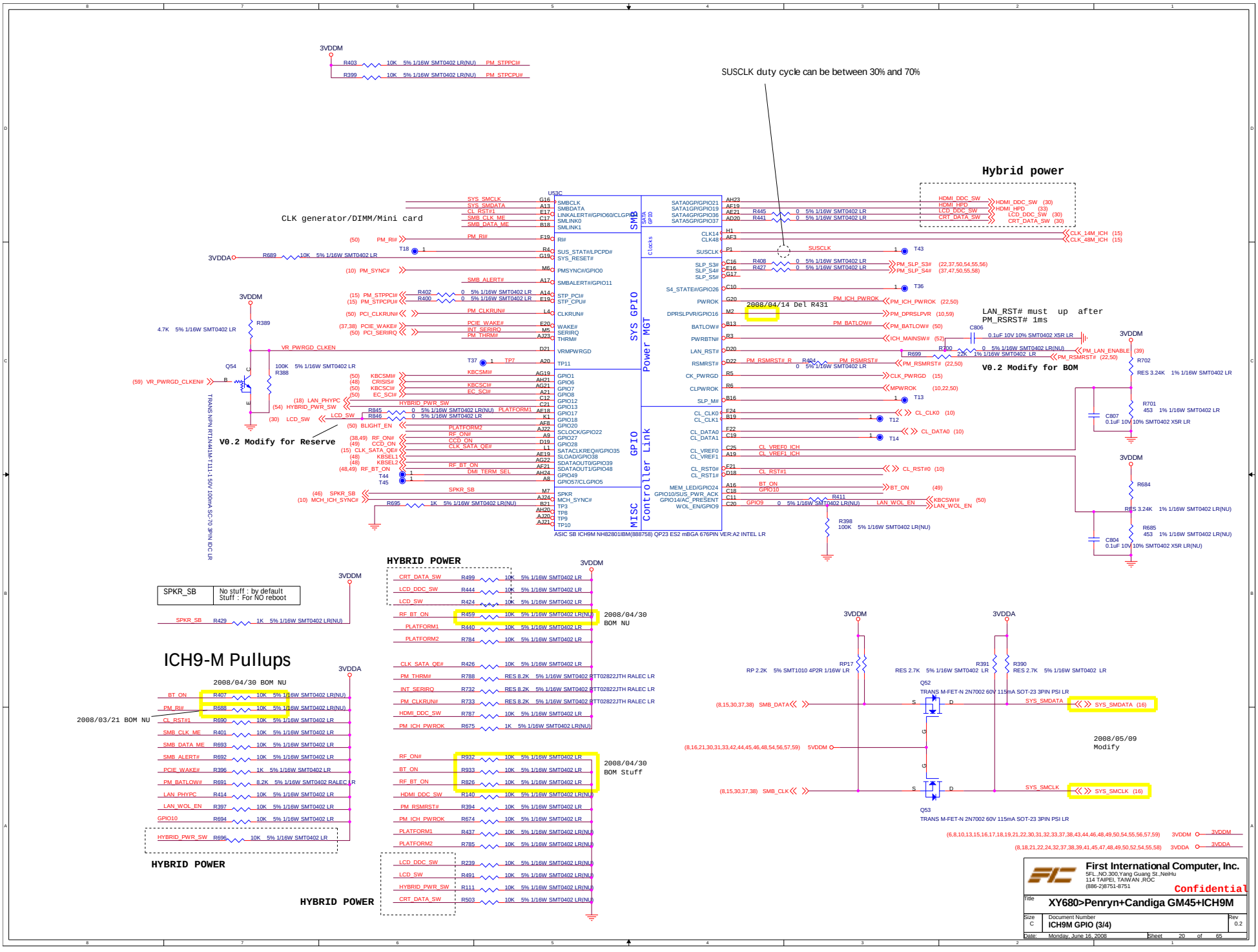
Title	XY680>Penryn+Candiga GM45+ICH9M
Size	C
Document Number	ICH9M CPU/IDE/SATA (2/4)
Rev	0.2
Date:	Monday, June 16, 2008
Sheet	19 of 65


CLK generator/DIMM/Mini card
SUSCLK duty cycle can be between 30% and 70%
Hybrid power
2008/04/14 Del R431
LAN_RST# must up after PM_RSRST# 1ms
V0.2 Modify for BOM
V0.2 Modify for Reserve
ASIC SB ICH9M NH82801IBM(888758) QP23 ES2 mBGA 676PIN VER:A2 INTEL LR
SPKR_SB
No stuff : by default
Stuff : For NO reboot
ICH9-M Pullups
2008/04/30 BOM NU
2008/03/21 BOM NU
2008/04/30 BOM Stuff
2008/05/09 Modify
HYBRID POWER
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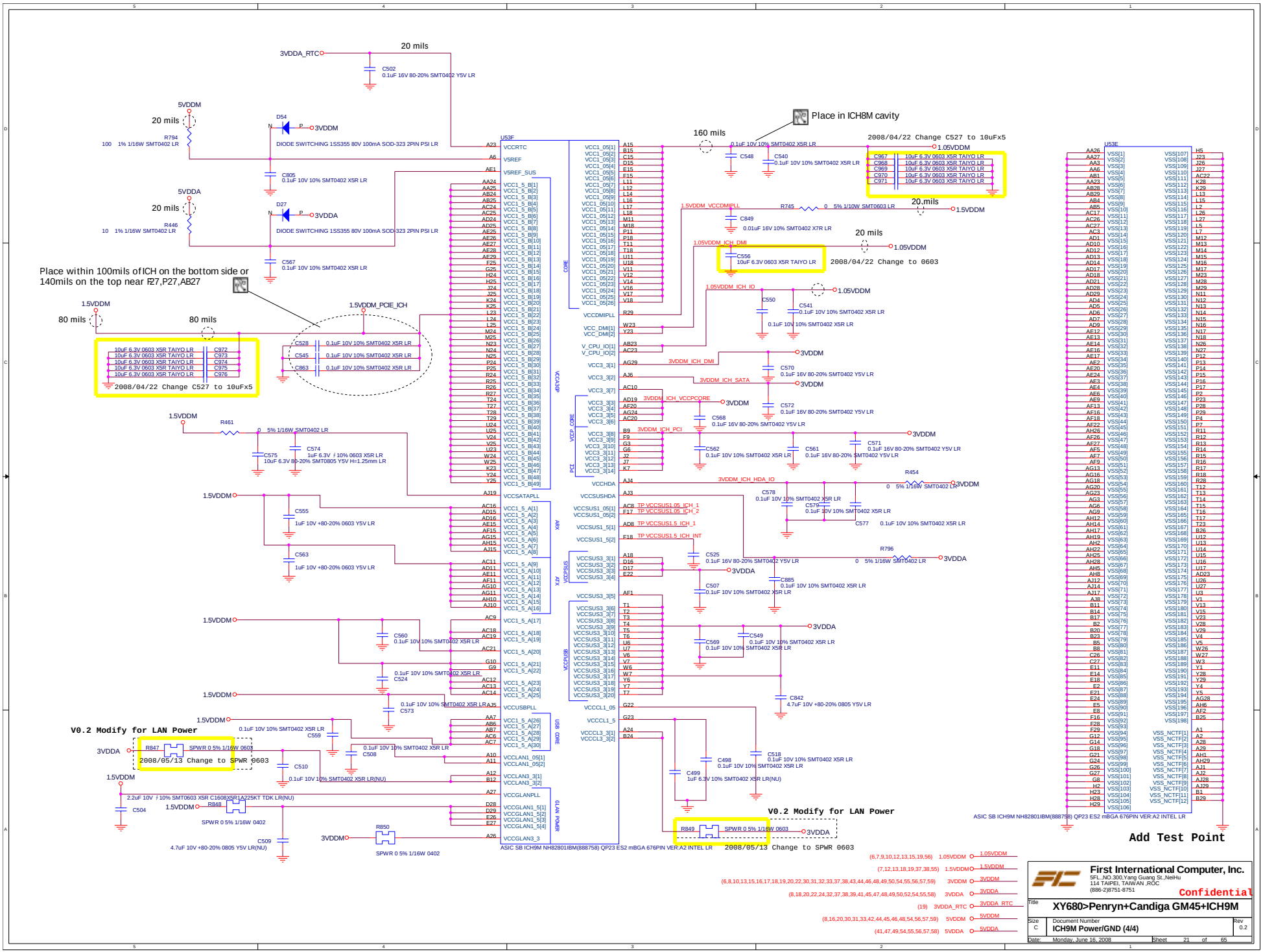
XY680>Penryn+Candiga GM45+ICH9M
ICH9M GPIO (3/4)
Monday, June 16, 2008


3VDDA_RTC
20 mils
C502
0.1uF 16V 80-20% SMT0402 Y5V LR
5VDDM
20 mils
R794
100 1% 1/16W SMT0402 LR
D54
3VDDM
DIODE SWITCHING 1SS355 80V 100mA SOD-323 2PIN PSI LR
C805
0.1uF 10V 10% SMT0402 X5R LR
5VDDA
20 mils
R446
10 1% 1/16W SMT0402 LR
D27
3VDDA
DIODE SWITCHING 1SS355 80V 100mA SOD-323 2PIN PSI LR
C567
0.1uF 10V 10% SMT0402 X5R LR
Place within 100mils of ICH on the bottom side or
140mils on the top near R27,P27,AB27
1.5VDDM
80 mils
80 mils
1.5VDDM_PCIE_ICH
10uF 6.3V 0603 X5R TAIYO LR C972
10uF 6.3V 0603 X5R TAIYO LR C973
10uF 6.3V 0603 X5R TAIYO LR C974
10uF 6.3V 0603 X5R TAIYO LR C975
10uF 6.3V 0603 X5R TAIYO LR C976
2008/04/22 Change C527 to 10uFx5
C528 0.1uF 10V 10% SMT0402 X5R LR
C545 0.1uF 10V 10% SMT0402 X5R LR
C863 0.1uF 10V 10% SMT0402 X5R LR
U53F
VCCRTC
V5REF
V5REF_SUS
VCC1_5_B[1]
VCC1_5_B[2]
VCC1_5_B[3]
VCC1_5_B[4]
VCC1_5_B[5]
VCC1_5_B[6]
VCC1_5_B[7]
VCC1_5_B[8]
VCC1_5_B[9]
VCC1_5_B[10]
VCC1_5_B[11]
VCC1_5_B[12]
VCC1_5_B[13]
VCC1_5_B[14]
VCC1_5_B[15]
VCC1_5_B[16]
VCC1_5_B[17]
VCC1_5_B[18]
VCC1_5_B[19]
VCC1_5_B[20]
VCC1_5_B[21]
VCC1_5_B[22]
VCC1_5_B[23]
VCC1_5_B[24]
VCC1_5_B[25]
VCC1_5_B[26]
VCC1_5_B[27]
VCC1_5_B[28]
VCC1_5_B[29]
VCC1_5_B[30]
VCC1_5_B[31]
VCC1_5_B[32]
VCC1_5_B[33]
VCC1_5_B[34]
VCC1_5_B[35]
VCC1_5_B[36]
VCC1_5_B[37]
VCC1_5_B[38]
VCC1_5_B[39]
VCC1_5_B[40]
VCC1_5_B[41]
VCC1_5_B[42]
VCC1_5_B[43]
VCC1_5_B[44]
VCC1_5_B[45]
VCC1_5_B[46]
VCC1_5_B[47]
VCC1_5_B[48]
VCC1_5_B[49]
VCCSATAPLL
VCC1_5_A[1]
VCC1_5_A[2]
VCC1_5_A[3]
VCC1_5_A[4]
VCC1_5_A[5]
VCC1_5_A[6]
VCC1_5_A[7]
VCC1_5_A[8]
VCC1_5_A[9]
VCC1_5_A[10]
VCC1_5_A[11]
VCC1_5_A[12]
VCC1_5_A[13]
VCC1_5_A[14]
VCC1_5_A[15]
VCC1_5_A[16]
VCC1_5_A[17]
VCC1_5_A[18]
VCC1_5_A[19]
VCC1_5_A[20]
VCC1_5_A[21]
VCC1_5_A[22]
VCC1_5_A[23]
VCC1_5_A[24]
VCC1_5_A[25]
VCCUSBPLL
VCC1_5_A[26]
VCC1_5_A[27]
VCC1_5_A[28]
VCC1_5_A[29]
VCC1_5_A[30]
VCCLAN1_05[1]
VCCLAN1_05[2]
VCCLAN3_3[1]
VCCLAN3_3[2]
VCCGLANPLL
VCCGLAN1_5[1]
VCCGLAN1_5[2]
VCCGLAN1_5[3]
VCCGLAN1_5[4]
VCCGLAN3_3
CORE
VCCA3GP
VCCP_CORE
PCI
AUX
VCCP5USB
VCCP1USB
USB CORE
GLAN POWER
ASIC SB ICH9M NH82801IBM(888758) QP23 ES2 mBGA 676PIN VER:A2 INTEL LR
R461
0 5% 1/16W SMT0402 LR
C574
1uF 6.3V 10% 0603 X5R LR
C575
10uF 6.3V 80-20% SMT0805 Y5V H=1.25mm LR
C555
1uF 10V +80-20% 0603 Y5V LR
C563
1uF 10V +80-20% 0603 Y5V LR
C560
0.1uF 10V 10% SMT0402 X5R LR
C524
0.1uF 10V 10% SMT0402 X5R LR
C573
0.1uF 10V 10% SMT0402 X5R LR
V0.2 Modify for LAN Power
0.1uF 10V 10% SMT0402 X5R LR
C559
3VDDA
R847
SPWR 0.5% 1/16W 0603
2008/05/13 Change to SPWR 0603
C510
0.1uF 10V 10% SMT0402 X5R LR(NU)
C508
0.1uF 10V 10% SMT0402 X5R LR
1.5VDDM
2.2uF 10V 10% SMT0603 X5R C1608X5R1A225KT TDK LR(NU)
C504
1.5VDDM
R848
SPWR 0 5% 1/16W 0402
C509
4.7uF 10V +80-20% 0805 Y5V LR(NU)
3VDDM
R850
SPWR 0 5% 1/16W 0402
Place in ICH8M cavity
160 mils
0.1uF 10V 10% SMT0402 X5R LR
C548
C540
0.1uF 10V 10% SMT0402 X5R LR
2008/04/22 Change C527 to 10uFx5
1.05VDDM
C967 10uF 6.3V 0603 X5R TAIYO LR
C968 10uF 6.3V 0603 X5R TAIYO LR
C969 10uF 6.3V 0603 X5R TAIYO LR
C970 10uF 6.3V 0603 X5R TAIYO LR
C971 10uF 6.3V 0603 X5R TAIYO LR
20 mils
1.5VDDM_VCCDMIPLL
R745
0 5% 1/10W SMT0603 LR
1.5VDDM
C849
0.01uF 16V 10% SMT0402 X7R LR
20 mils
1.05VDDM_ICH_DMI
1.05VDDM
C556
10uF 6.3V 0603 X5R TAIYO LR
2008/04/22 Change to 0603
1.05VDDM_ICH_IO
1.05VDDM
C550
C541
0.1uF 10V 10% SMT0402 X5R LR
0.1uF 10V 10% SMT0402 X5R LR
3VDDM_ICH_DMI
3VDDM
C570
0.1uF 16V 80-20% SMT0402 Y5V LR
3VDDM_ICH_SATA
3VDDM
C572
0.1uF 16V 80-20% SMT0402 Y5V LR
3VDDM_ICH_VCCPCORE
3VDDM
C568
0.1uF 16V 80-20% SMT0402 Y5V LR
3VDDM_ICH_PCI
3VDDM
C562
0.1uF 10V 10% SMT0402 X5R LR
C561
0.1uF 16V 80-20% SMT0402 Y5V LR
C571
0.1uF 16V 80-20% SMT0402 Y5V LR
3VDDM_ICH_HDA_IO
R454
0 5% 1/16W SMT0402 LR
3VDDM
C578
0.1uF 10V 10% SMT0402 X5R LR
C579
0.1uF 10V 10% SMT0402 X5R LR
C577
0.1uF 10V 10% SMT0402 X5R LR
TP_VCCSUS1.05_ICH_1
TP_VCCSUS1.05_ICH_2
TP_VCCSUS1.5_ICH_1
TP_VCCSUS1.5_ICH_INT
C525
0.1uF 16V 80-20% SMT0402 Y5V LR
3VDDA
R796
0 5% 1/16W SMT0402 LR
3VDDA
C507
0.1uF 10V 10% SMT0402 X5R LR
C885
0.1uF 10V 10% SMT0402 X5R LR
3VDDA
C549
0.1uF 10V 10% SMT0402 X5R LR
C569
0.1uF 10V 10% SMT0402 X5R LR
C842
4.7uF 10V +80-20% 0805 Y5V LR
C498
0.1uF 10V 10% SMT0402 X5R LR
C518
0.1uF 10V 10% SMT0402 X5R LR
C499
1uF 6.3V 10% SMT0402 X5R LR(NU)
V0.2 Modify for LAN Power
R849
SPWR 0.5% 1/16W 0603
3VDDA
2008/05/13 Change to SPWR 0603
U53E
VSS[1]
VSS[2]
VSS[3]
VSS[4]
VSS[5]
VSS[6]
VSS[7]
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VSS[192]
VSS[193]
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VSS[196]
VSS[197]
VSS[198]
VSS_NCTF[1]
VSS_NCTF[2]
VSS_NCTF[3]
VSS_NCTF[4]
VSS_NCTF[5]
VSS_NCTF[6]
VSS_NCTF[7]
VSS_NCTF[8]
VSS_NCTF[9]
VSS_NCTF[10]
VSS_NCTF[11]
VSS_NCTF[12]
ASIC SB ICH9M NH82801IBM(888758) QP23 ES2 mBGA 676PIN VER:A2 INTEL LR
Add Test Point
(6,7,9,10,12,13,15,19,56) 1.05VDDM
(7,12,13,18,19,37,38,55) 1.5VDDM
(6,8,10,13,15,16,17,18,19,20,22,30,31,32,33,37,38,43,44,46,48,49,50,54,55,56,57,59) 3VDDM
(8,18,20,22,24,32,37,38,39,41,45,47,48,49,50,52,54,55,58) 3VDDA
(19) 3VDDA_RTC
(8,16,20,30,31,33,42,44,45,46,48,54,56,57,59) 5VDDM
(41,47,49,54,55,56,57,58) 5VDDA
1.05VDDM
1.5VDDM
3VDDM
3VDDA
3VDDA_RTC
5VDDM
5VDDA
First International Computer, Inc.
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Title
XY680>Penryn+Candiga GM45+ICH9M
Size C
Document Number
ICH9M Power/GND (4/4)
Rev 0.2
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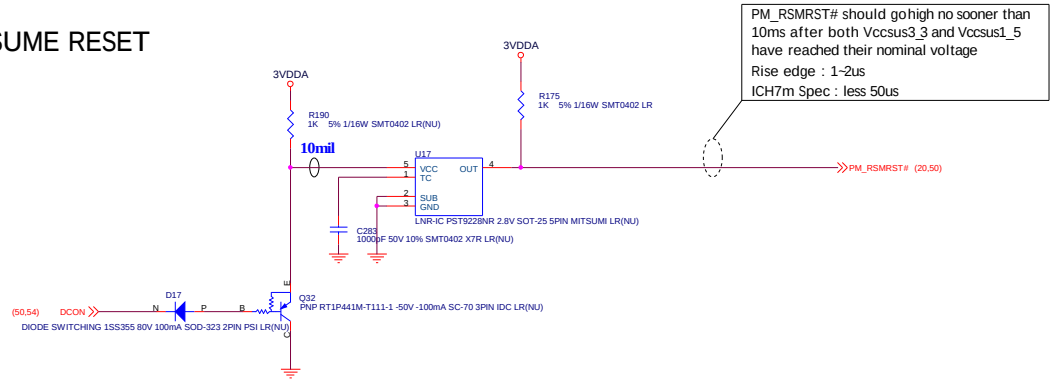
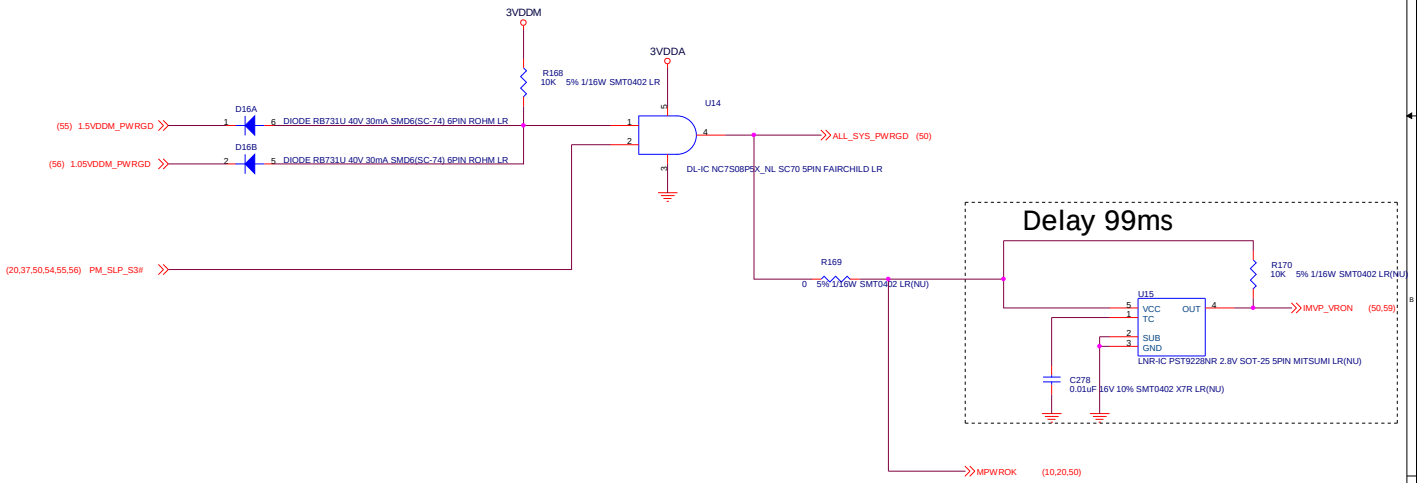
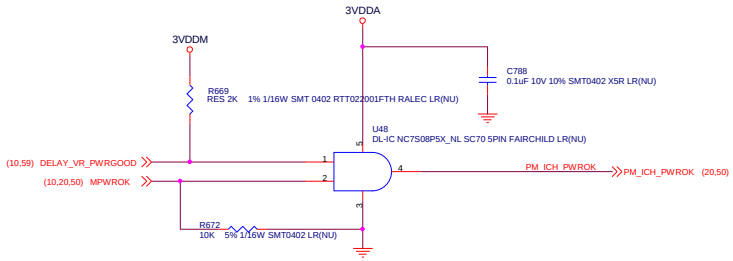
RESUME RESET



Montevina Platfoem Power Good Circuit





(6,8,10,13,15,16,17,18,19,20,21,30,31,32,33,37,38,43,44,46,48,49,50,54,55,56,57,59) 3VDDM 3VDDM

(8,18,20,21,24,32,37,38,39,41,45,47,48,49,50,52,54,55,58) 3VDDA 3VDDA

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Size: C | Document Number: Reset Circuit | Rev: 0.2

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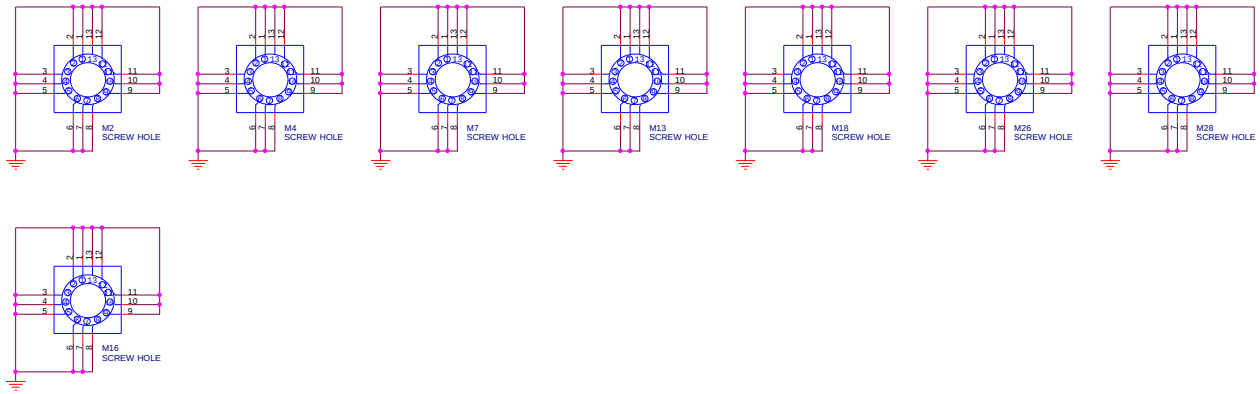
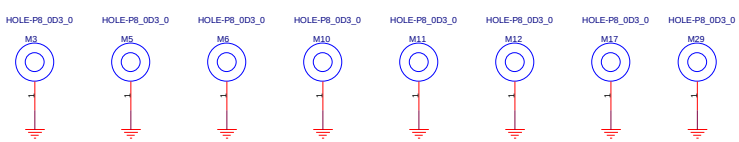
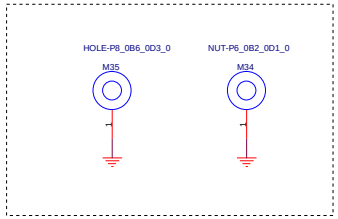
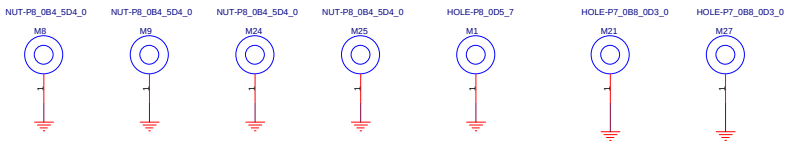
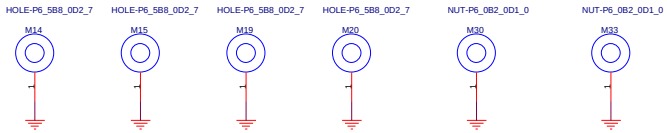


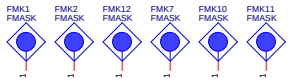


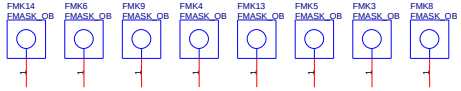


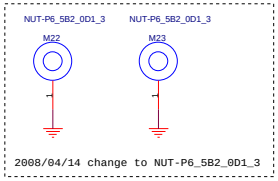
V0.2 Modify for 18"







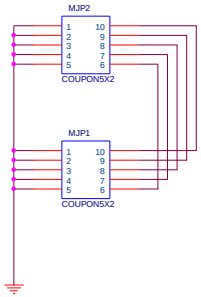




V0.2 Modify

2008/04/14 change to NUT-P6_5B2_0D1_3

COUPON 5X2



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Title: XY680>Penryn+Candiga GM45+ICH9M

Size: C | Document Number: Screw Hole | Rev: 0.2

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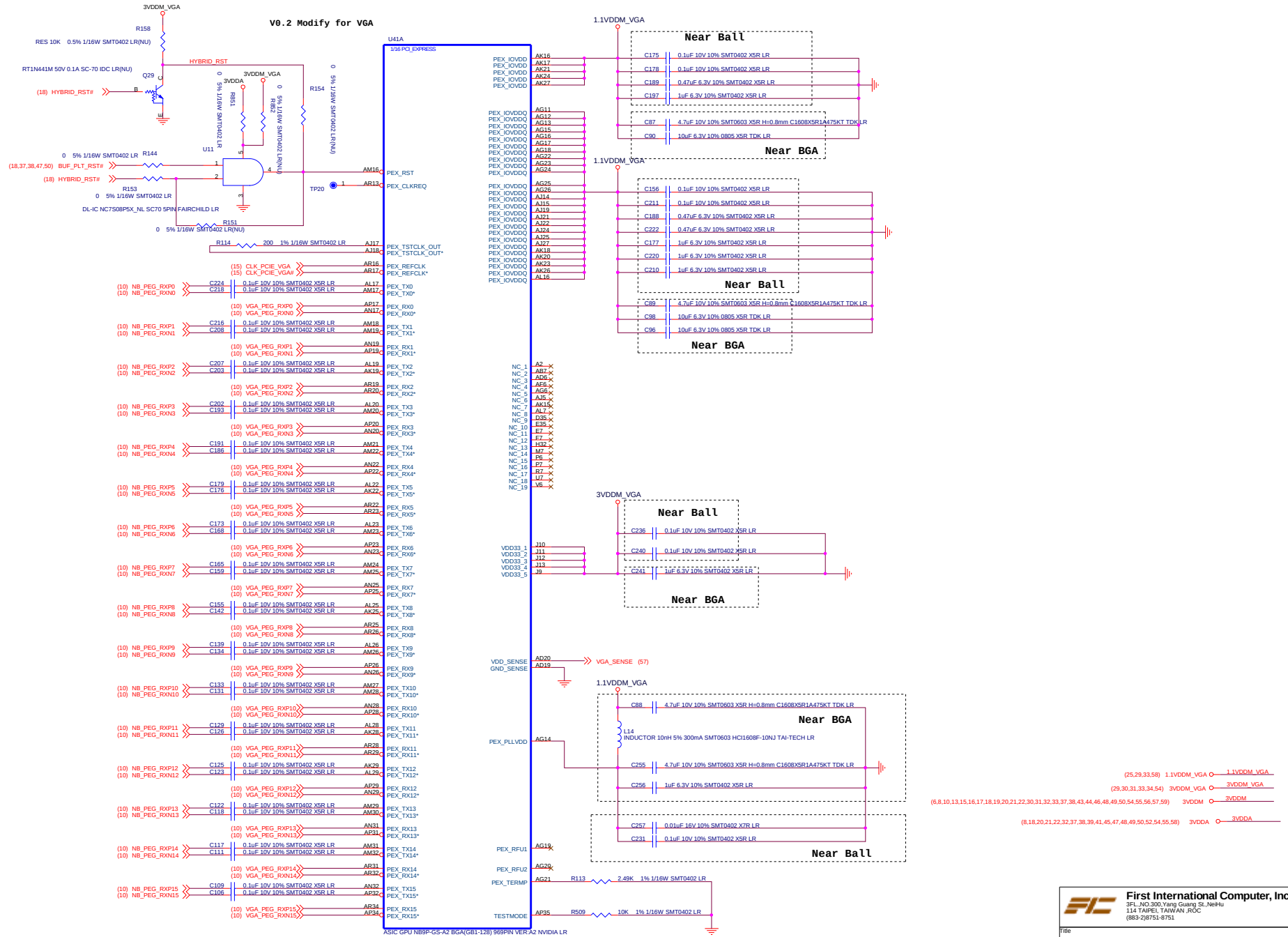
V0.2 Modify for VGA
U41A
1/16 PCI_EXPRESS
ASIC GPU NB9P-GS-A2 BGA(GB1-128) 969PIN VER:A2 NVIDIA LR
3VDDM_VGA
R158
RES 10K 0.5% 1/16W SMT0402 LR(NU)
HYBRID_RST
RT1N441M 50V 0.1A SC-70 IDC LR(NU)
Q29
(18) HYBRID_RST#
3VDDA
R154
R151
R152
5% 1/16W SMT0402 LR(NU)
U11
R144
(18,37,38,47,50) BUF_PLT_RST#
R153
DL-IC NC7S08P5X_NL SC70 5PIN FAIRCHILD LR
R151
TP20
AM16 PEX_RST
AR13 PEX_CLKREQ
R114 200 1% 1/16W SMT0402 LR
AJ17 PEX_TSTCLK_OUT
AJ18 PEX_TSTCLK_OUT*
(15) CLK_PCIE_VGA
(15) CLK_PCIE_VGA#
AR16 PEX_REFCLK
AR17 PEX_REFCLK*
1.1VDDM_VGA
Near Ball
C175 0.1uF 10V 10% SMT0402 X5R LR
C178 0.1uF 10V 10% SMT0402 X5R LR
C189 0.47uF 6.3V 10% SMT0402 X5R LR
C197 1uF 6.3V 10% SMT0402 X5R LR
C87 4.7uF 10V 10% SMT0603 X5R H=0.8mm C1608X5R1A475KT TDK LR
C90 10uF 6.3V 10% 0805 X5R TDK LR
Near BGA
C156 0.1uF 10V 10% SMT0402 X5R LR
C211 0.1uF 10V 10% SMT0402 X5R LR
C188 0.47uF 6.3V 10% SMT0402 X5R LR
C222 0.47uF 6.3V 10% SMT0402 X5R LR
C177 1uF 6.3V 10% SMT0402 X5R LR
C220 1uF 6.3V 10% SMT0402 X5R LR
C210 1uF 6.3V 10% SMT0402 X5R LR
C89 4.7uF 10V 10% SMT0603 X5R H=0.8mm C1608X5R1A475KT TDK LR
C98 10uF 6.3V 10% 0805 X5R TDK LR
C96 10uF 6.3V 10% 0805 X5R TDK LR
3VDDM_VGA
C236 0.1uF 10V 10% SMT0402 X5R LR
C240 0.1uF 10V 10% SMT0402 X5R LR
C241 1uF 6.3V 10% SMT0402 X5R LR
VGA_SENSE (57)
C88 4.7uF 10V 10% SMT0603 X5R H=0.8mm C1608X5R1A475KT TDK LR
L14
INDUCTOR 10nH 5% 300mA SMT0603 HCI1608F-10NJ TAI-TECH LR
C255 4.7uF 10V 10% SMT0603 X5R H=0.8mm C1608X5R1A475KT TDK LR
C256 1uF 6.3V 10% SMT0402 X5R LR
C257 0.01uF 16V 10% SMT0402 X7R LR
C231 0.1uF 10V 10% SMT0402 X5R LR
R113 2.49K 1% 1/16W SMT0402 LR
R509 10K 1% 1/16W SMT0402 LR
(25,29,33,58) 1.1VDDM_VGA
(29,30,31,33,34,54) 3VDDM_VGA
(6,8,10,13,15,16,17,18,19,20,21,22,30,31,32,33,37,38,43,44,46,48,49,50,54,55,56,57,59) 3VDDM
(8,18,20,21,22,32,37,38,39,41,45,47,48,49,50,52,54,55,58) 3VDDA
First International Computer, Inc.
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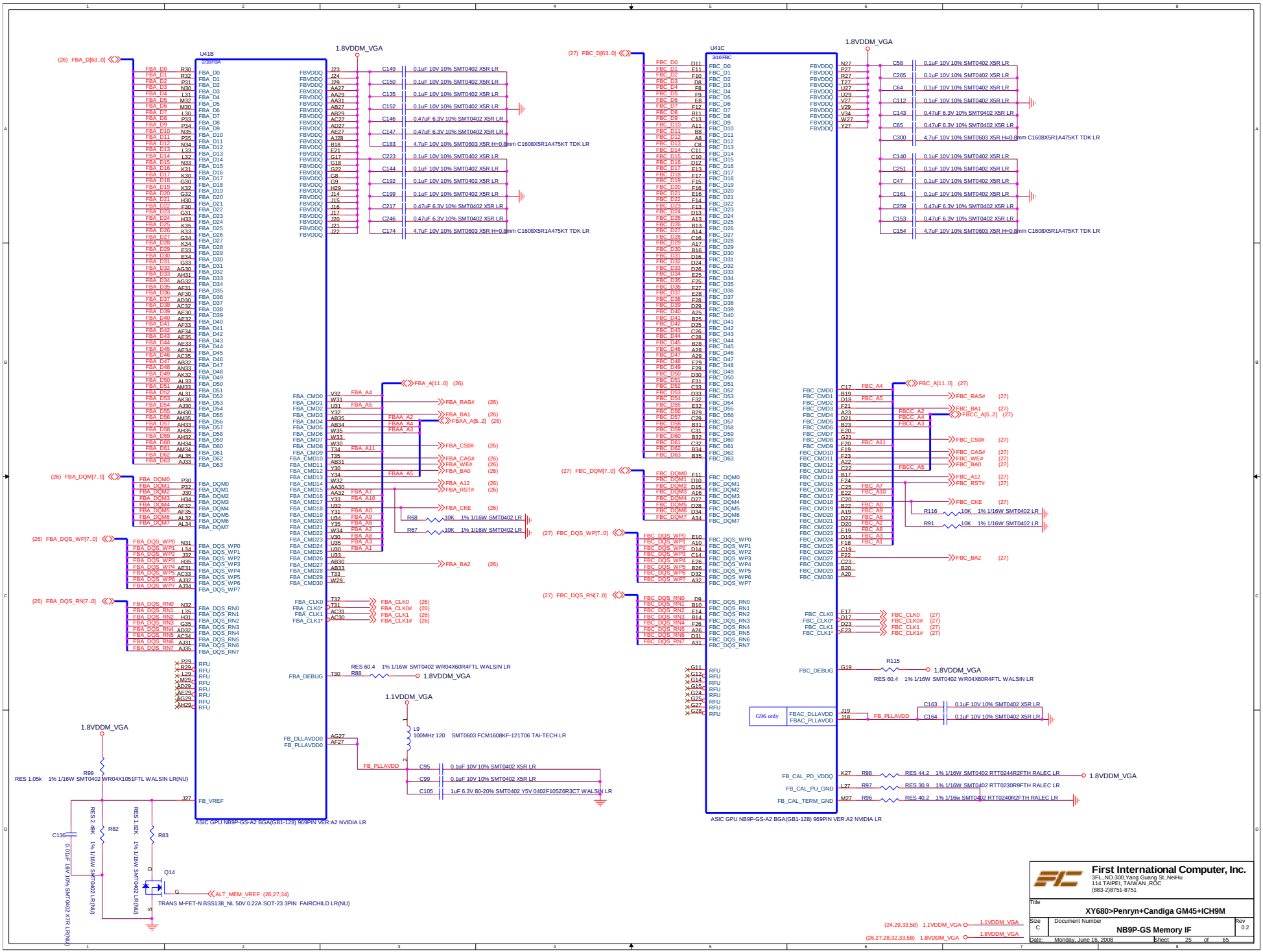
114 TAIPEI, TAIWAN ,ROC
(883-2)8751-8751
XY680>Penryn+Candiga GM45+ICH9M
NB9P-GS PCI-E IF
Size C
Rev 0.2
Date: Monday, June 16, 2008
Sheet 24 of 65



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Title	XY680>Penryn+Candiga GM45+ICH9M
Size	C
Document Number	NB9P-GS Memory IF
Rev	0.2
Date	Monday, June 16, 2008
Sheet	25 of 65

(24,29,33,58) 1.1VDDM_VGA
(26,27,28,32,33,58) 1.8VDDM_VGA

Samsung 16Mx32 | 02-41059-01

1 0 2 3

4 5 7 6

50mil

1000mA

1.8VDDM_VGA

U36

U37

GDDR3 SDRAM HYB18H1G321AF-11 1Gbit(4M*32bit*8banks) 1.8V PG-TFBGA 136PIN QIMONDA LR

Low sets the non-mirror mode

High sets the mirror mode

R47 RES 475 1% 1/16W SMT0402 LR

R55 RES 475 1% 1/16W SMT0402 LR

R52 243 1% 1/16W SMT0402 LR

R49 243 1% 1/16W SMT0402 LR

R50 0 5% 1/16W SMT0402 LR

R51 0 5% 1/16W SMT0402 LR

C71 MO-CAP 0.047uF 16V ±10% SMT0402 X5R 0402X473K160CT WALSIN LR

C36 MO-CAP 0.047uF 16V ±10% SMT0402 X5R 0402X473K160CT WALSIN LR

C79 MO-CAP 0.047uF 16V ±10% SMT0402 X5R 0402X473K160CT WALSIN LR

C35 MO-CAP 0.047uF 16V ±10% SMT0402 X5R 0402X473K160CT WALSIN LR

R44 RES 549 1% 1/16W SMT0402 LR

R57 RES 549 1% 1/16W SMT0402 LR

R56 RES 549 1% 1/16W SMT0402 LR

R43 RES 549 1% 1/16W SMT0402 LR

RES 931 1% 1/16W SMT0402 LR

RES 1.33K 1% 1/16W SMT0402 RM04FTN1331 TA-I LR

C34 0.01uF 16V 10% SMT0402 X7R LR

C86 0.01uF 16V 10% SMT0402 X7R LR

C84 0.01uF 16V 10% SMT0402 X7R LR

C33 0.01uF 16V 10% SMT0402 X7R LR

Q5 TRANS M-FET-N BSS138_NL 50V 0.22A SOT-23 3PIN FAIRCHILD LR

Q10 TRANS M-FET-N BSS138_NL 50V 0.22A SOT-23 3PIN FAIRCHILD LR

Q9 TRANS M-FET-N BSS138_NL 50V 0.22A SOT-23 3PIN FAIRCHILD LR

Q4 TRANS M-FET-N BSS138_NL 50V 0.22A SOT-23 3PIN FAIRCHILD LR

ALT_MEM_VREF (25,27,34)

(25,27,28,32,33,58) 1.8VDDM_VGA

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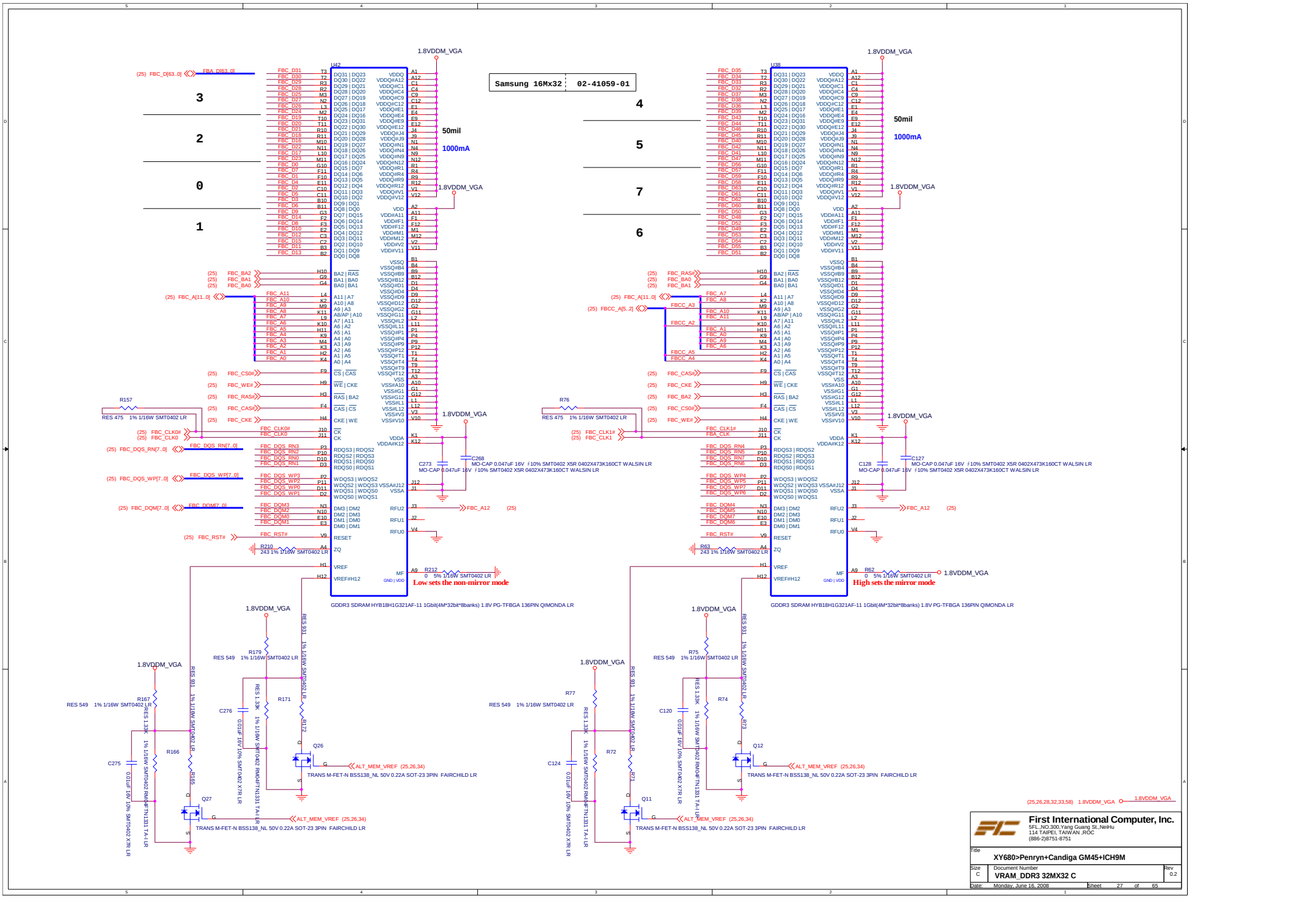
Title: XY680>Penryn+Candiga GM45+ICH9M

Size: C | Document Number: VRAM_DDR3 32MX32 A | Rev: 0.2

Date: Monday, June 16, 2008 | Sheet 26 of 65


Samsung 16Mx32 | 02-41059-01
1.8VDDM_VGA
50mil
1000mA
U42
U38
GDDR3 SDRAM HYB18H1G321AF-11 1Gbit(4M*32bit*8banks) 1.8V PG-TFBGA 136PIN QIMONDA LR
Low sets the non-mirror mode
High sets the mirror mode
TRANS M-FET-N BSS138_NL 50V 0.22A SOT-23 3PIN FAIRCHILD LR
ALT_MEM_VREF (25,26,34)
First International Computer, Inc.
5FL.,NO.300,Yang Guang St.,NeiHu
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XY680>Penryn+Candiga GM45+ICH9M
VRAM_DDR3 32MX32 C
Monday, June 16, 2008
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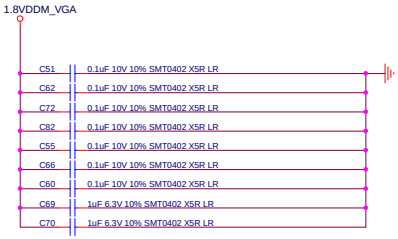
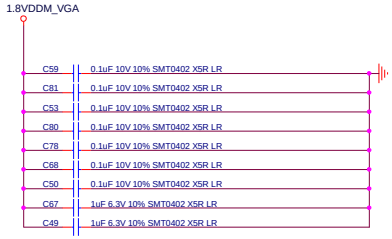
FBA MEMORY DECOUPLING

DECOUPLING BENEATH F BA (DQ0 - DQ31)

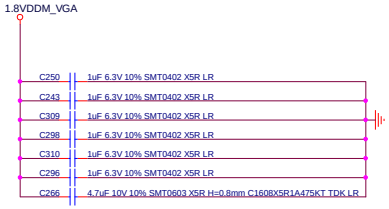
DECOUPLING BENEATH FB A (DQ32 - DQ63)



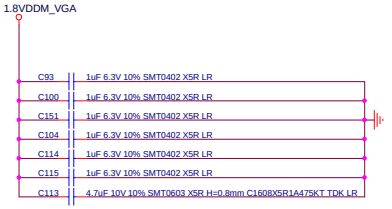


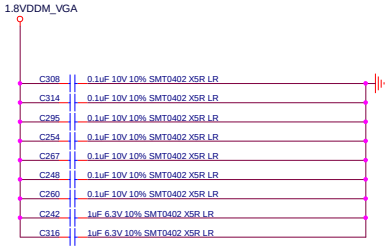
FBC MEMORY DECOUPLING

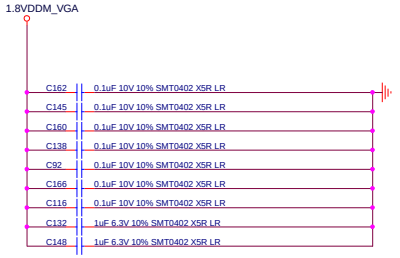
DECOUPLING BENEATH F BC (DQ0 - DQ31)



DECOUPLING BENEATH FB C (DQ32 - DQ63)







(25,26,27,32,33,58) 1.8VDDM_VGA 1.8VDDM_VGA

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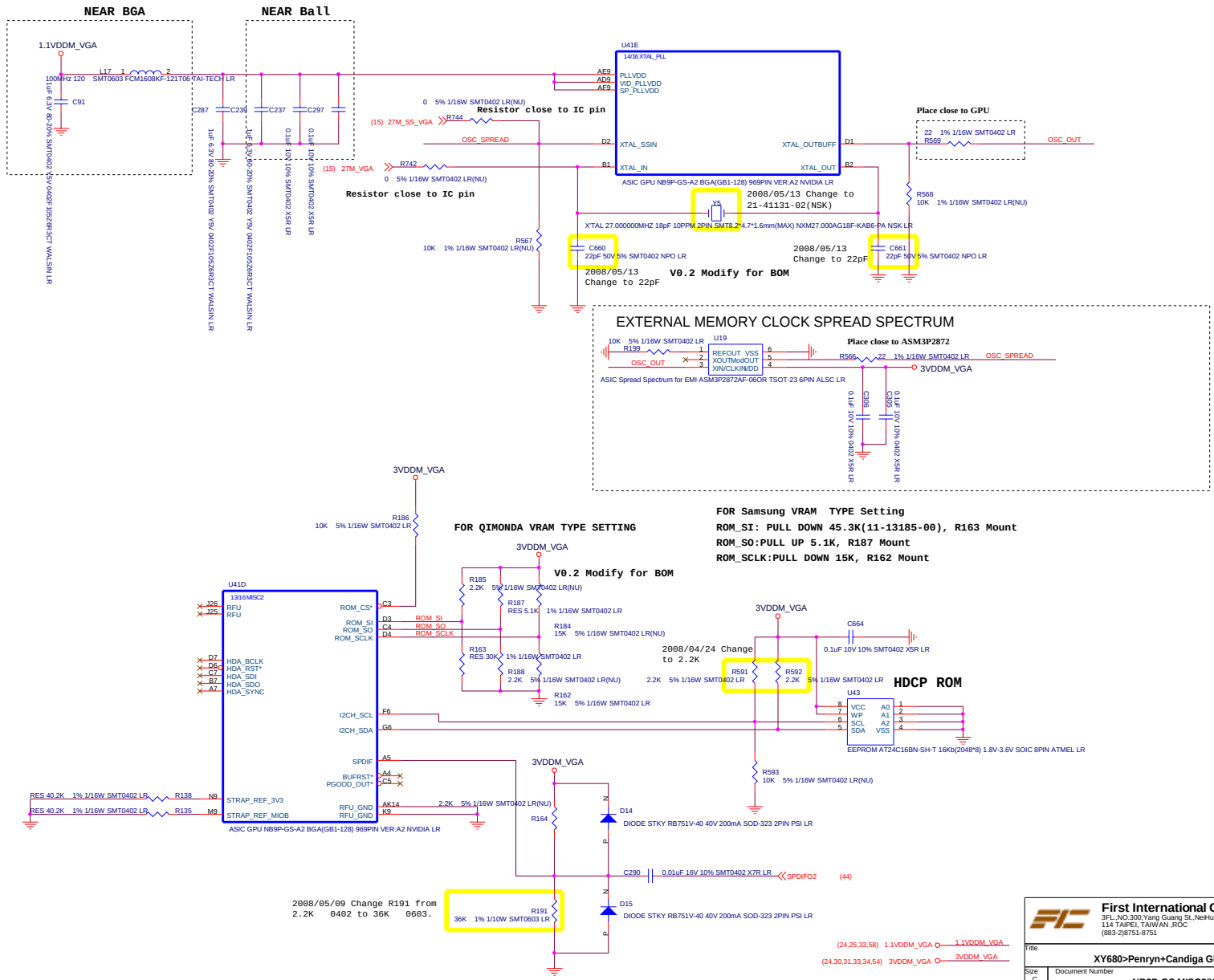
Title	XY680>Penryn+Candiga GM45+ICH9M	
Size C	Document Number FBA/C MEMORY DECOUPLING	Rev 0.2
Date: Monday, June 16, 2008	Sheet 28 of 65	



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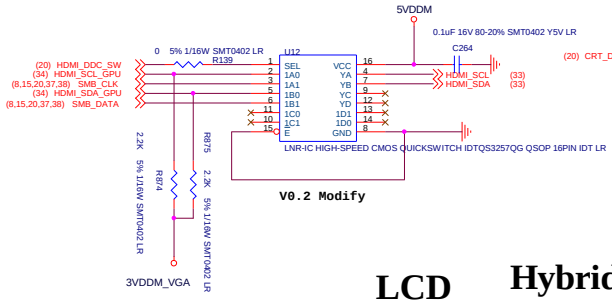
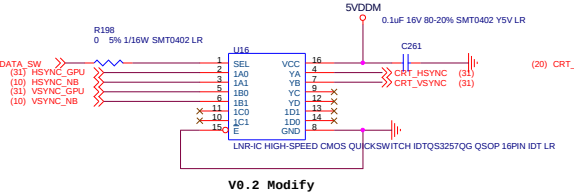
Title	XY680>Penryn+Candiga GM45+ICH9M
Size C	Document Number NB9P-GS MISC2/XTAL_PLL Rev 0.2
Date: Monday, June 16, 2008	Sheet 29 of 65

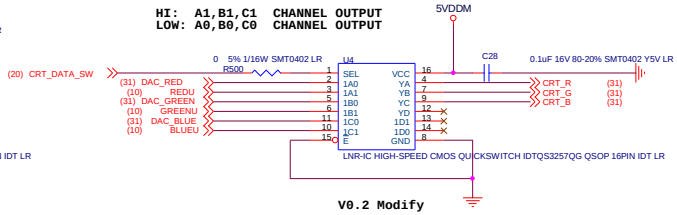
HDMI DDC SW



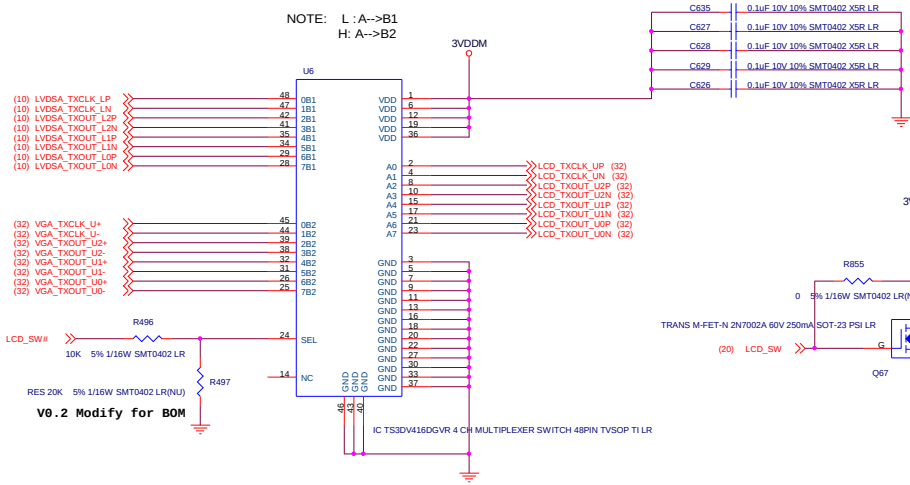
CRT/HSYNC/VSYNC

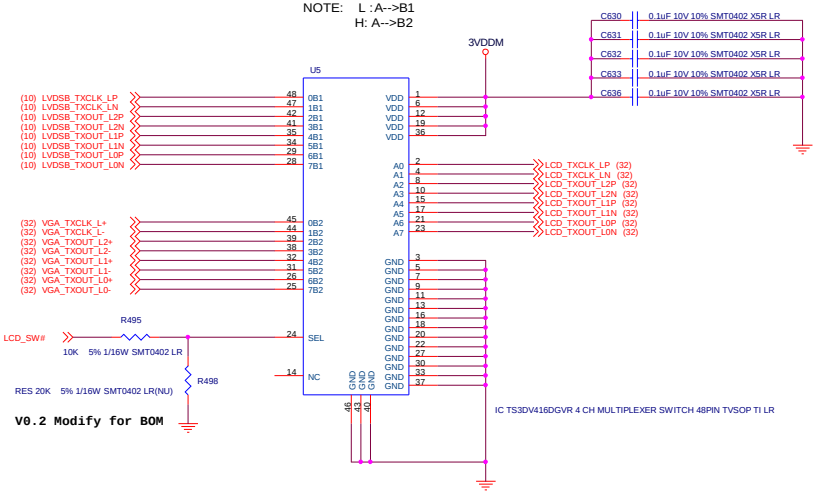


CRT/R/G/B

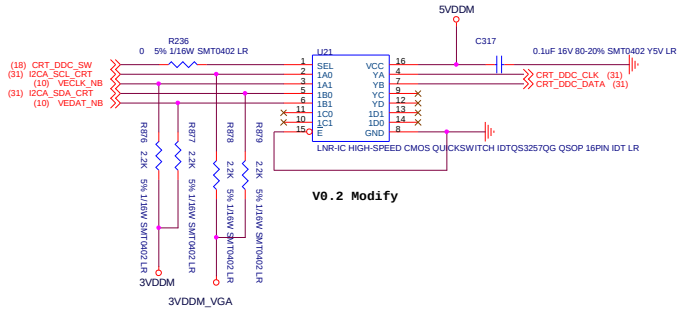


LCD Hybrid Power

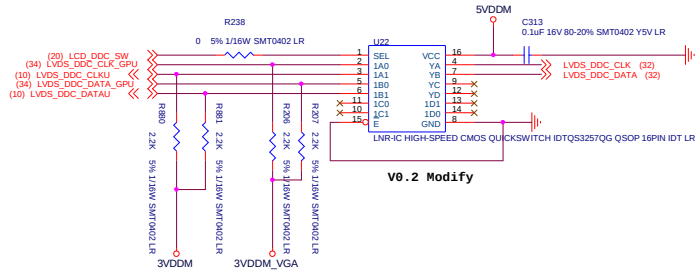




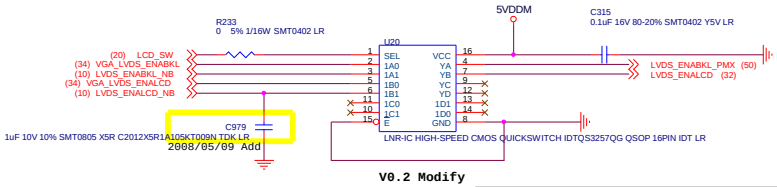
CRT DDC SW



LCD DDC SW



LVDS Blanklight and VCC



(24,29,31,33,34,54) 3VDDM_VGA — 3VDDM_VGA
(8,16,20,21,31,33,42,44,45,46,48,54,56,57,59) 5VDDM — 5VDDM
(6,8,10,13,15,16,17,18,19,20,21,22,31,32,33,37,38,43,44,46,48,49,50,54,55,56,57,59) 3VDDM — 3VDDM

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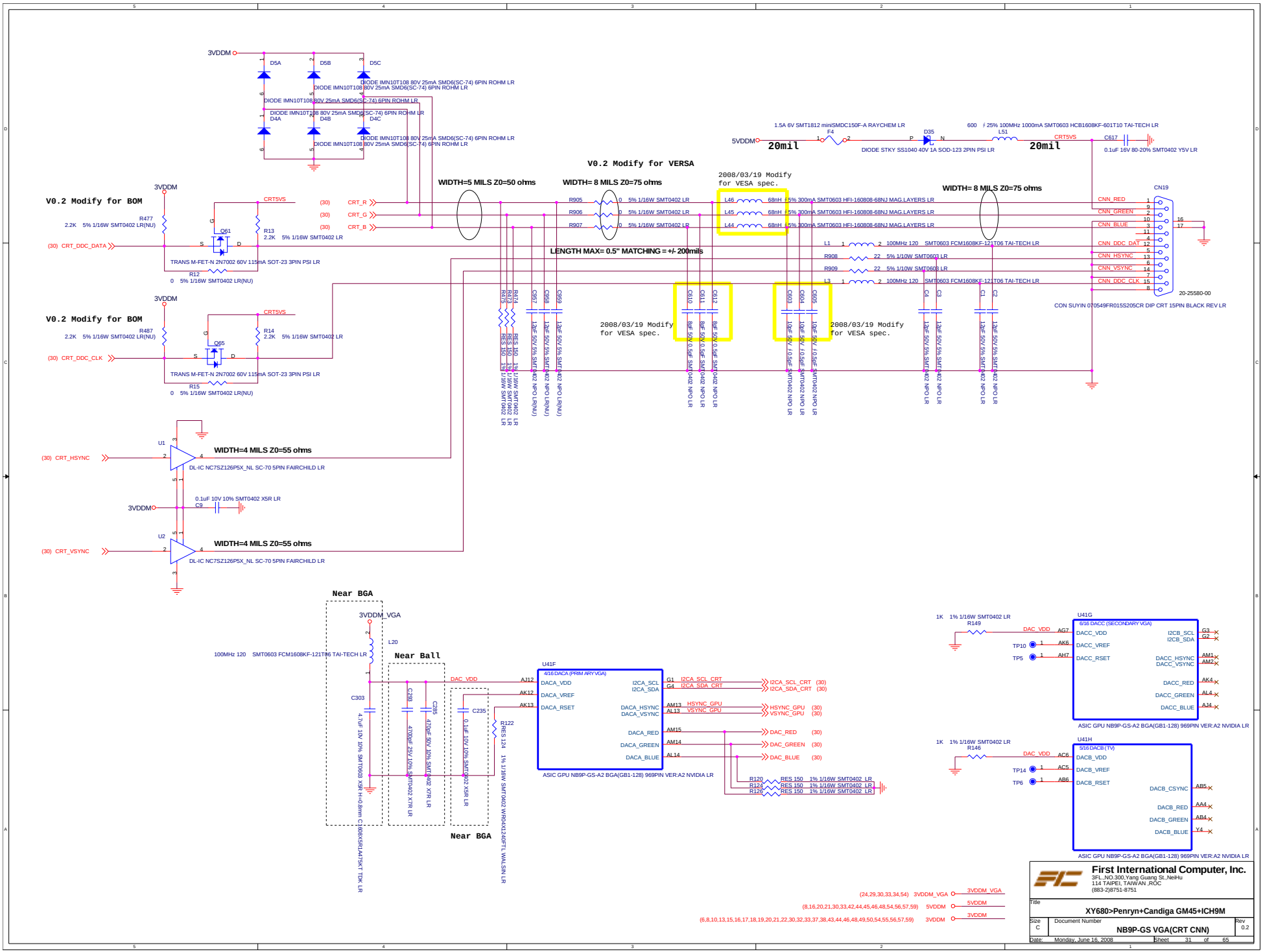
Title: XY680>Penryn+Candiga GM45+ICH9M

Size: C | Document Number: Hybrid Power SWITCH | Rev: 0.2

Date: Monday, June 16, 2008 | Sheet 30 of 65



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Title	XY680>Penryn+Candiga GM45+ICH9M
Size	C
Document Number	NB9P-GS VGA(CRT CNN)
Rev	0.2
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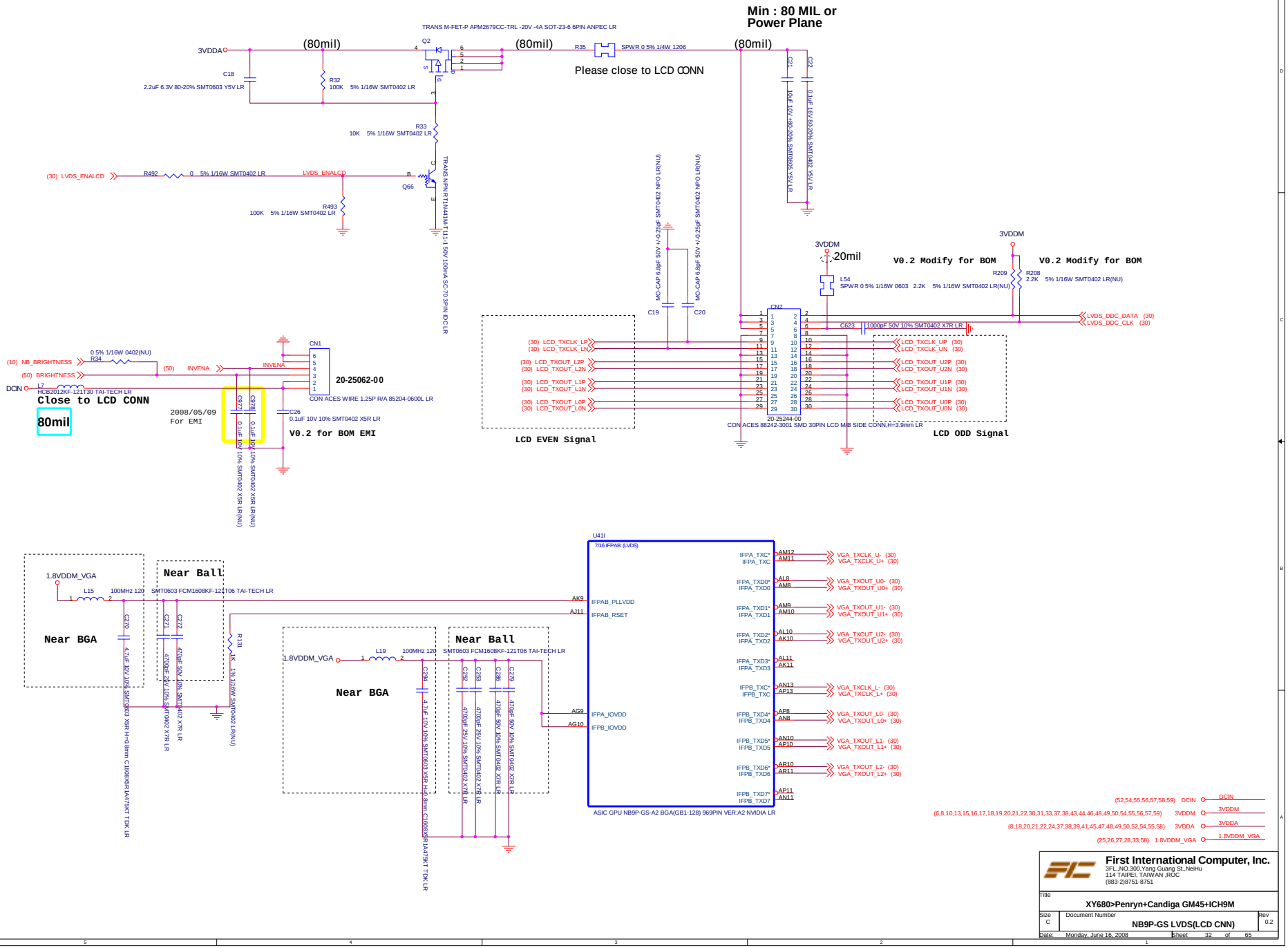
Min : 80 MIL or Power Plane
TRANS M-FET-P APM2679CC-TRL -20V -4A SOT-23-6 6PIN ANPEC LR
3VDDA
(80mil)
Q2
(80mil)
R35
SPWR 0 5% 1/4W 1206
(80mil)
Please close to LCD CONN
C18
2.2uF 6.3V 80-20% SMT0603 Y5V LR
R32
100K 5% 1/16W SMT0402 LR
C21
C22
10uF 10V +80-20% SMT0805 Y5V LR
0.1uF 16V 80-20% SMT0402 Y5V LR
R33
10K 5% 1/16W SMT0402 LR
(30) LVDS_ENALCD
R492
0 5% 1/16W SMT0402 LR
LVDS_ENALCD
Q66
TRANS NPN RT1N441MT111-150V 100mA SC-70 3PIN IDC LR
R493
100K 5% 1/16W SMT0402 LR
MO-CAP 6.8pF 50V +/-0.25pF SMT0402 NPO LR(NU)
MO-CAP 6.8pF 50V +/-0.25pF SMT0402 NPO LR(NU)
C19
C20
3VDDM
20mil
V0.2 Modify for BOM
V0.2 Modify for BOM
R209
R208
2.2K 5% 1/16W SMT0402 LR(NU)
L54
SPWR 0 5% 1/16W 0603 2.2K 5% 1/16W SMT0402 LR(NU)
CN2
C623
1000pF 50V 10% SMT0402 X7R LR
LVDS_DDC_DATA (30)
LVDS_DDC_CLK (30)
(30) LCD_TXCLK_LP
(30) LCD_TXCLK_LN
LCD_TXCLK_UP (30)
LCD_TXCLK_UN (30)
(30) LCD_TXOUT_L2P
(30) LCD_TXOUT_L2N
LCD_TXOUT_U2P (30)
LCD_TXOUT_U2N (30)
(30) LCD_TXOUT_L1P
(30) LCD_TXOUT_L1N
LCD_TXOUT_U1P (30)
LCD_TXOUT_U1N (30)
(30) LCD_TXOUT_L0P
(30) LCD_TXOUT_L0N
LCD_TXOUT_U0P (30)
LCD_TXOUT_U0N (30)
20-25244-00
CON ACES 88242-3001 SMD 30PIN LCD MIB SIDE CONN,H=3.9mm LR
LCD EVEN Signal
LCD ODD Signal
(10) NB_BRIGHTNESS
0 5% 1/16W 0402(NU)
R34
(50) BRIGHTNESS
(50)
INVENA
INVENA
DCIN
L7
HCB2012KF-121T30 TAI-TECH LR
Close to LCD CONN
80mil
2008/05/09
For EMI
CN1
20-25062-00
CON ACES WIRE 1.25P R/A 85204-0600L LR
C277
0.1uF 10V 10% SMT0402 X5R LR(NU)
C278
0.1uF 10V 10% SMT0402 X5R LR(NU)
C26
0.1uF 10V 10% SMT0402 X5R LR
V0.2 for BOM EMI
U41I
7/16 IFPAB (LVDS)
AK9
IFPAB_PLLVDD
AJ11
IFPAB_RSET
IFPA_TXC*
IFPA_TXC
AM12
AM11
VGA_TXCLK_U- (30)
VGA_TXCLK_U+ (30)
IFPA_TXD0*
IFPA_TXD0
AL8
AM8
VGA_TXOUT_U0- (30)
VGA_TXOUT_U0+ (30)
IFPA_TXD1*
IFPA_TXD1
AM9
AM10
VGA_TXOUT_U1- (30)
VGA_TXOUT_U1+ (30)
IFPA_TXD2*
IFPA_TXD2
AL10
AK10
VGA_TXOUT_U2- (30)
VGA_TXOUT_U2+ (30)
IFPA_TXD3*
IFPA_TXD3
AL11
AK11
IFPB_TXC*
IFPB_TXC
AN13
AP13
VGA_TXCLK_L- (30)
VGA_TXCLK_L+ (30)
IFPB_TXD4*
IFPB_TXD4
AP8
AN8
VGA_TXOUT_L0- (30)
VGA_TXOUT_L0+ (30)
IFPB_TXD5*
IFPB_TXD5
AN10
AP10
VGA_TXOUT_L1- (30)
VGA_TXOUT_L1+ (30)
IFPB_TXD6*
IFPB_TXD6
AR10
AR11
VGA_TXOUT_L2- (30)
VGA_TXOUT_L2+ (30)
IFPB_TXD7*
IFPB_TXD7
AP11
AN11
AG9
IFPA_IOVDD
AG10
IFPB_IOVDD
ASIC GPU NB9P-GS-A2 BGA(GB1-128) 969PIN VER:A2 NVIDIA LR
1.8VDDM_VGA
L15
100MHz 120
SMT0603 FCM1608KF-121T06 TAI-TECH LR
Near BGA
Near Ball
C270
4.7uF 10V 10% SMT0603 X5R H=0.8mm C1608X5R1A475KT TDK LR
C271
4700pF 25V 10% SMT0402 X7R LR
C272
470pF 50V 10% SMT0402 X7R LR
R131
1K 1% 1/16W SMT0402 LR(NU)
1.8VDDM_VGA
L19
100MHz 120
Near BGA
Near Ball
C284
4.7uF 10V 10% SMT0603 X5R H=0.8mm C1608X5R1A475KT TDK LR
C282
4700pF 25V 10% SMT0402 X7R LR
C283
4700pF 25V 10% SMT0402 X7R LR
C285
470pF 50V 10% SMT0402 X7R LR
C279
470pF 50V 10% SMT0402 X7R LR
(52,54,55,56,57,58,59) DCIN
DCIN
(6,8,10,13,15,16,17,18,19,20,21,22,30,31,33,37,38,43,44,46,48,49,50,54,55,56,57,59) 3VDDM
3VDDM
(8,18,20,21,22,24,37,38,39,41,45,47,48,49,50,52,54,55,58) 3VDDA
3VDDA
(25,26,27,28,33,58) 1.8VDDM_VGA
1.8VDDM_VGA
First International Computer, Inc.
3FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(883-2)8751-8751
Title
XY680>Penryn+Candiga GM45+ICH9M
Size C
Document Number
NB9P-GS LVDS(LCD CNN)
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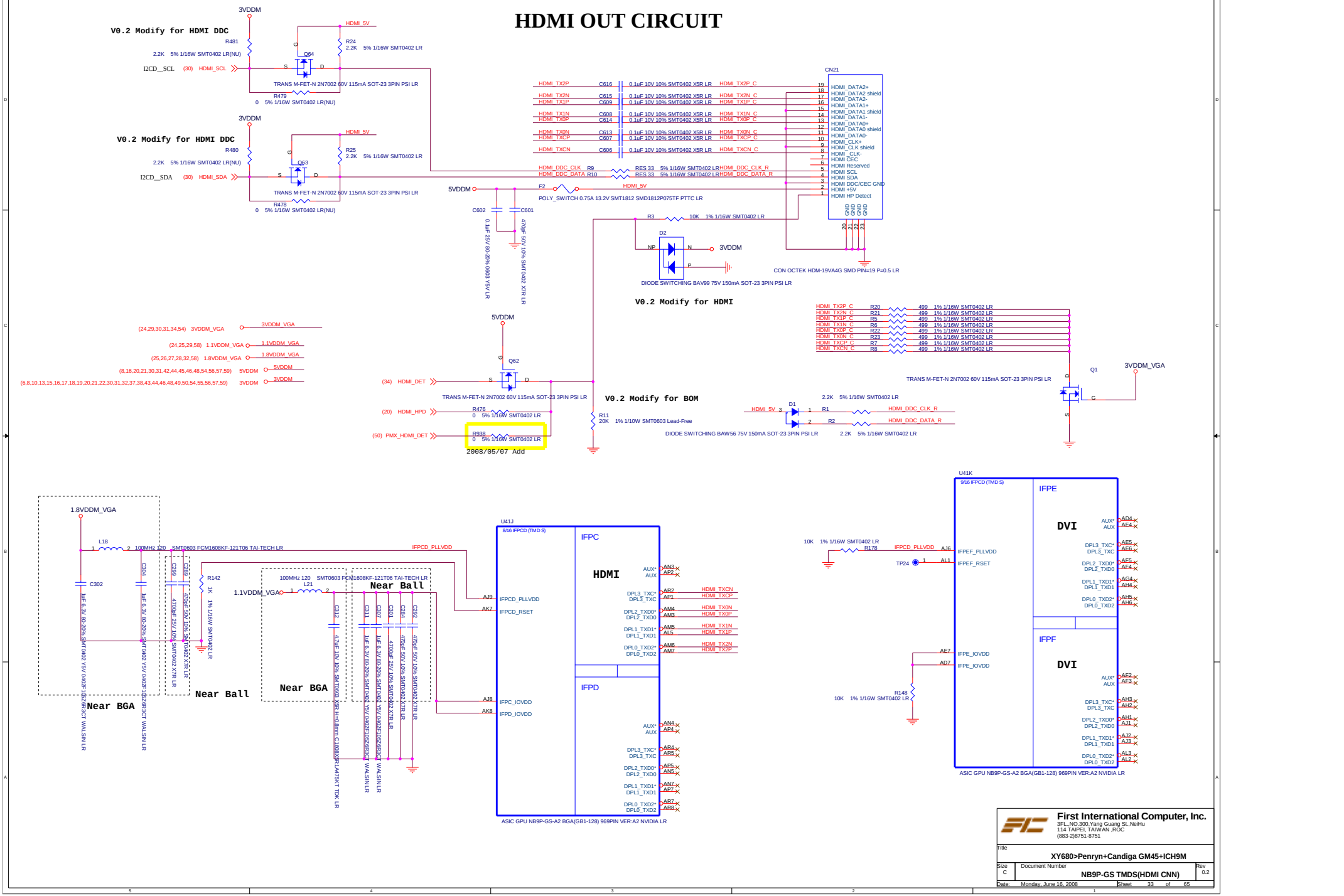
HDMI OUT CIRCUIT



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Title	XY680>Penryn+Candiga GM45+ICH9M	
Size C	Document Number NB9P-GS TMDS(HDMI CNN)	Rev 0.2
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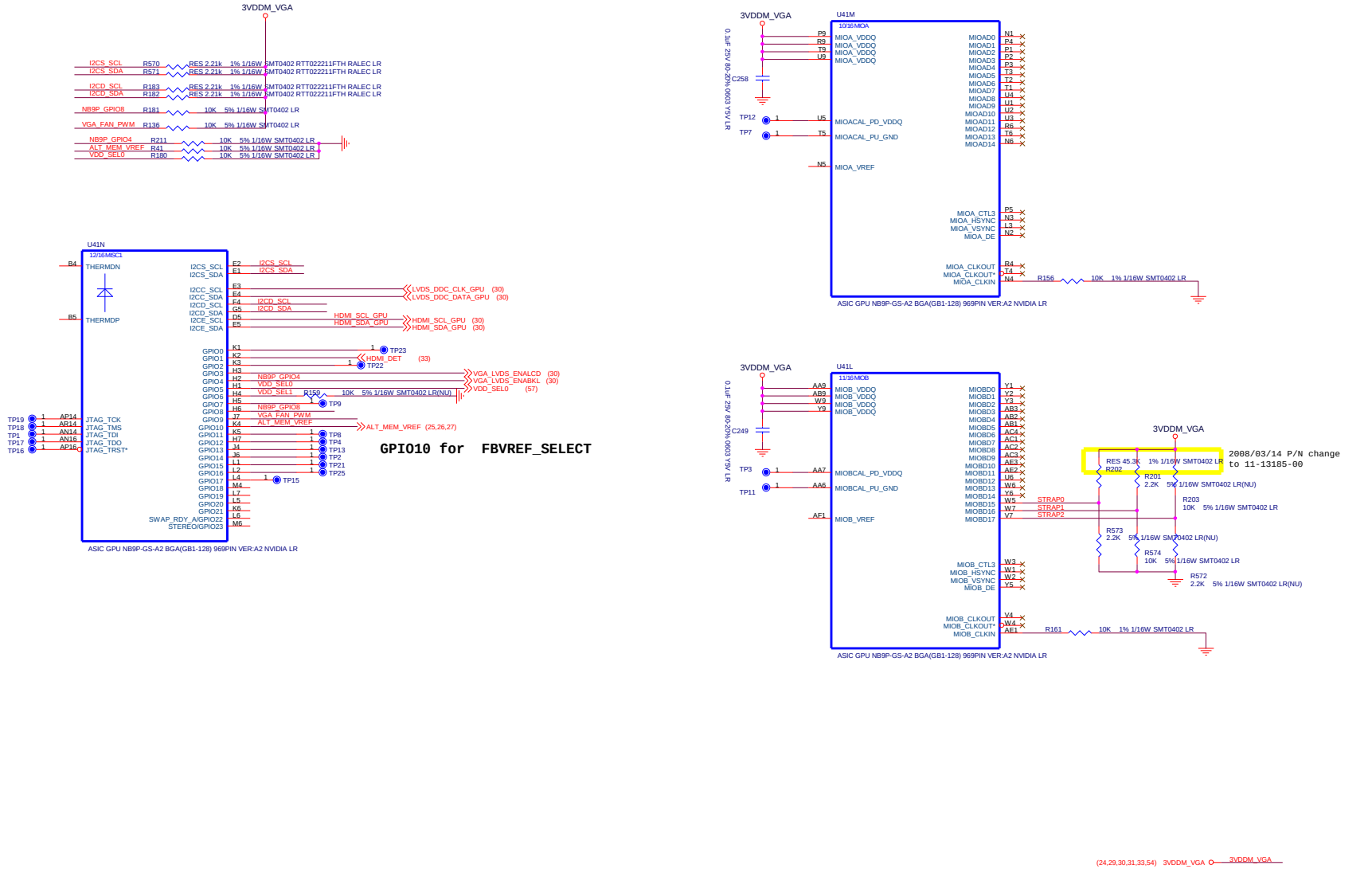

First International Computer, Inc.
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Title	XY680>Penryn+Candiga GM45+ICH9M
Size C	Document Number NB9P-GS MIOA/MIOB Rev 0.2
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Title: XY680>Penryn+Candiga GM45+ICH9M

Size: C | Document Number: NB9P-GS POWER/GND | Rev: 0.2

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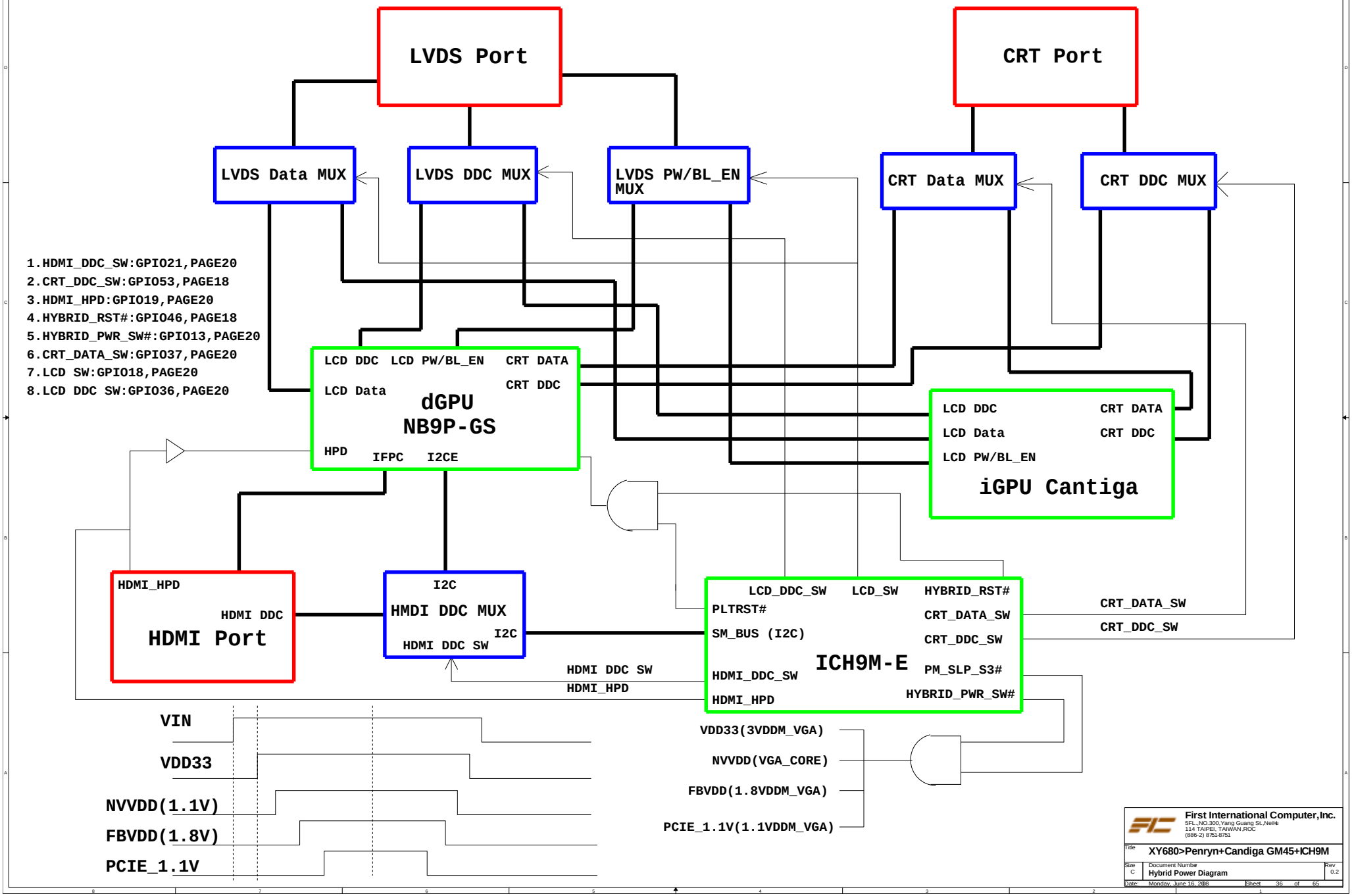
Hybrid power diagram for Montevina



First International Computer, Inc.
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Title	XY680>Penryn+Candiga GM45+ICH9M	
Size C	Document Number Hybrid Power Diagram	Rev 0.2
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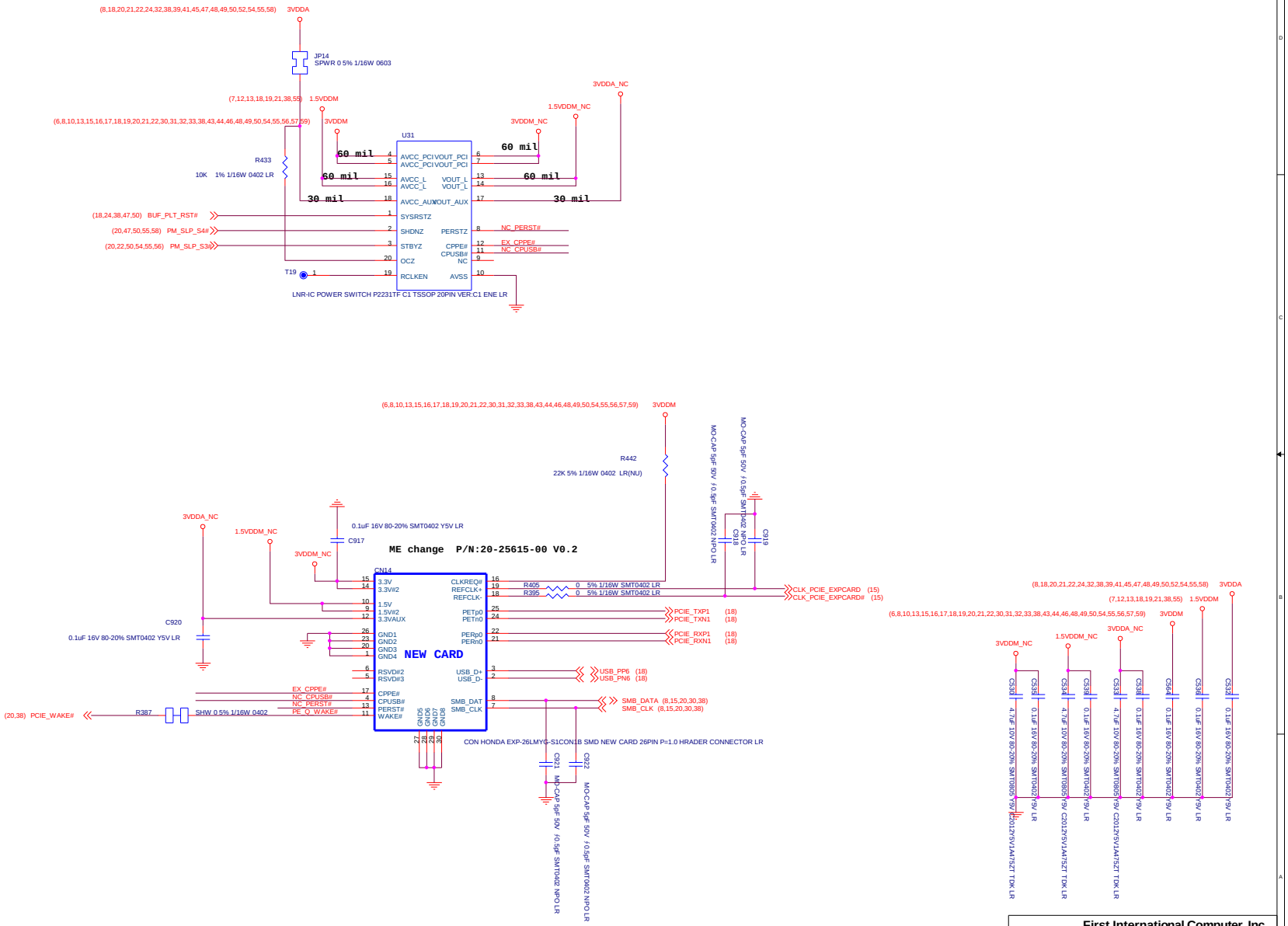

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2FL.,NO.300,Yang Guang St.,NeiHu	
114 TAIPEI, TAIWAN ,ROC	Confidential
(886-2)8751-8751	
Title	XY680>Penryn+Candiga GM45+ICH9M
Size C	Document Number: New Card(express card)
Rev	0.2
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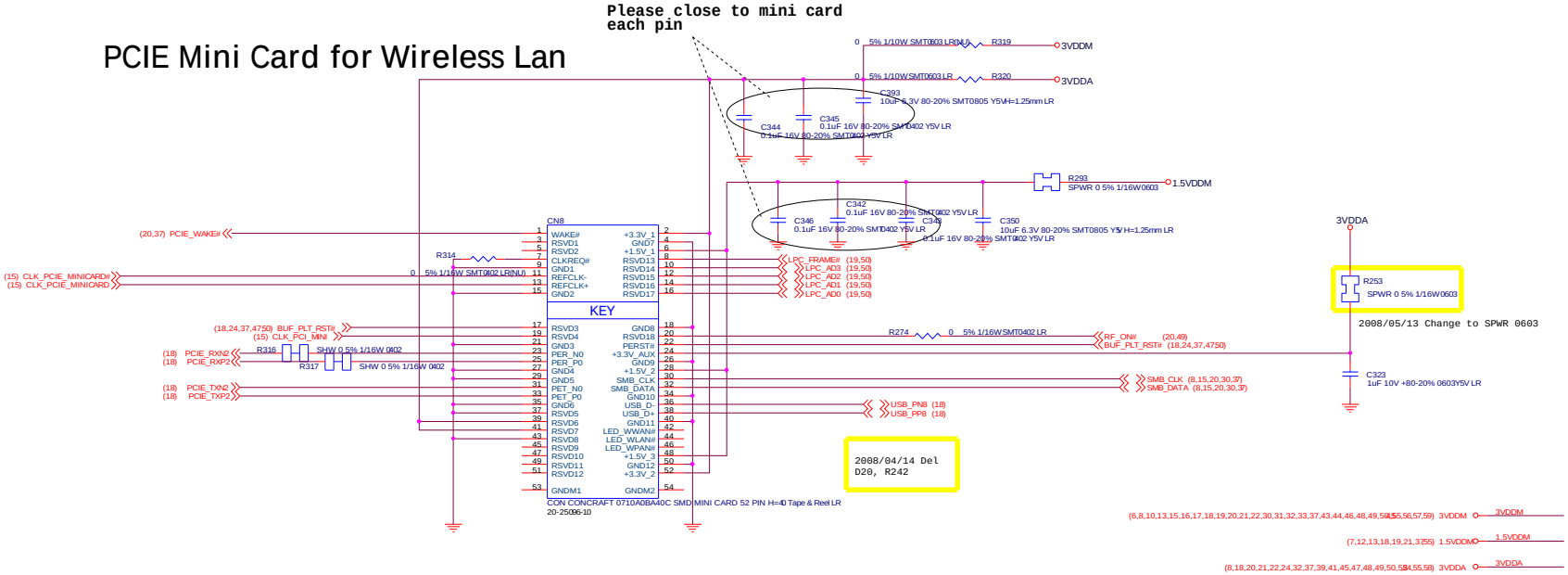
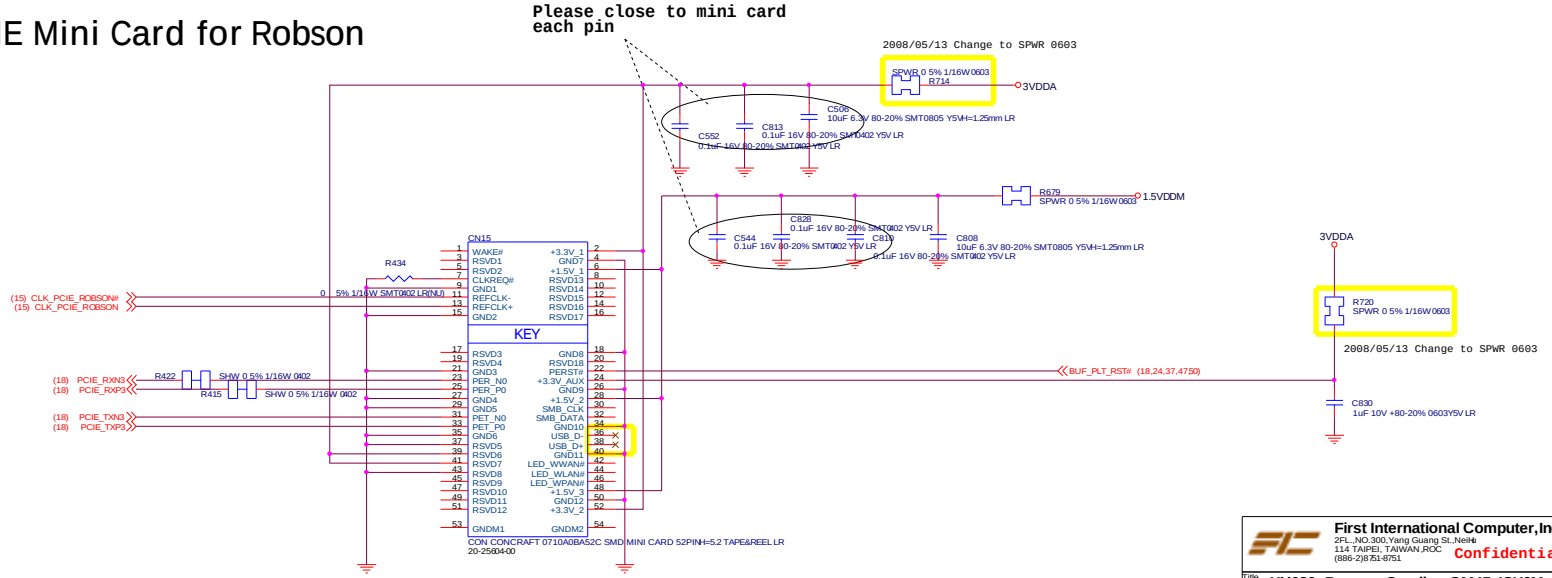
PCIE Mini Card for Wireless Lan



PCIE Mini Card for Robson



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Confidential

Title: XY680>Penryn+Candiga GM45+ICH9M

Size: C | Document Number: PCIE Mini Card WLAN/TV | Rev: 0.2

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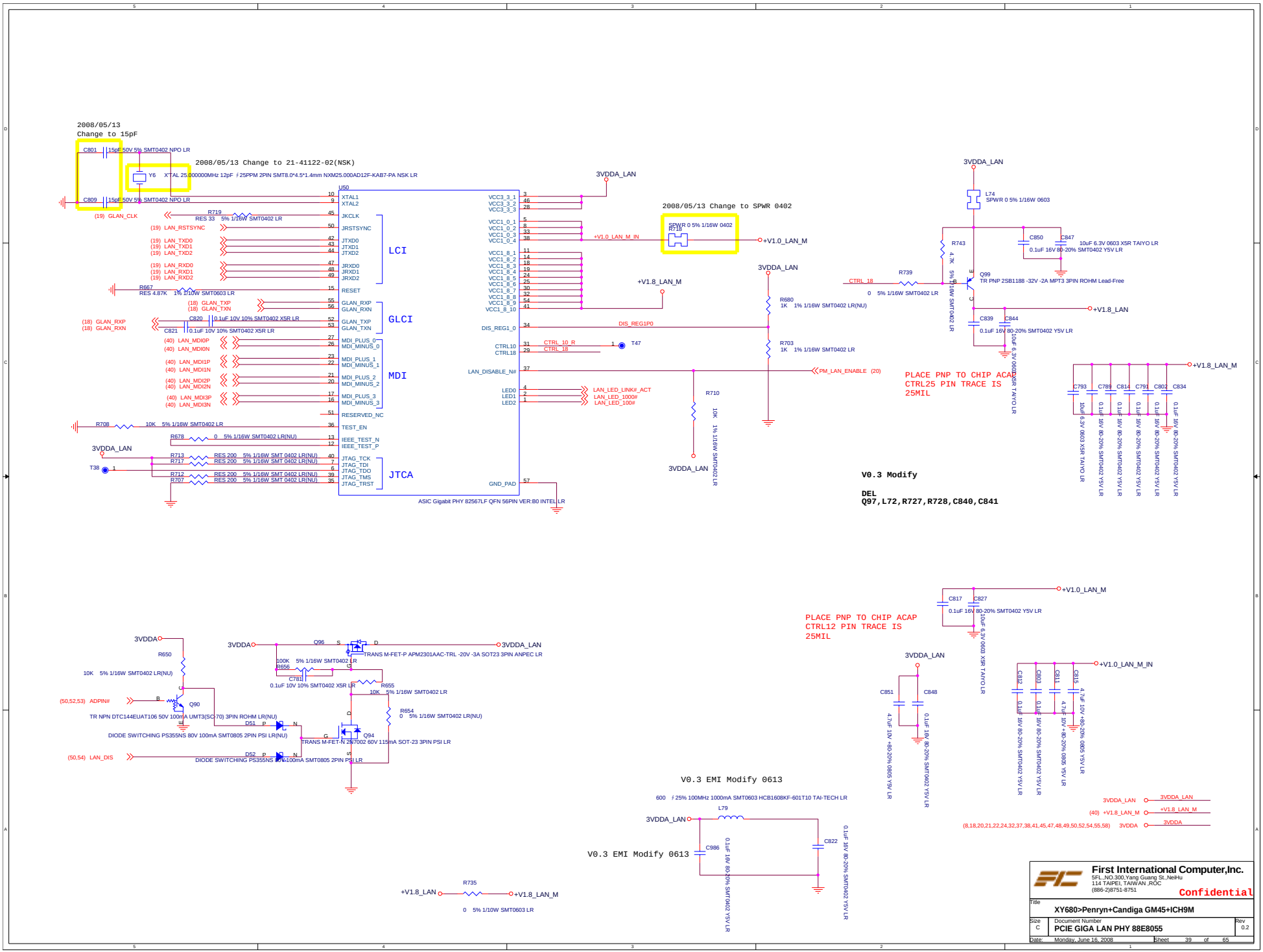
2008/05/13
Change to 15pF
C801 15pF 50V 5% SMT0402 NPO LR
C809 15pF 50V 5% SMT0402 NPO LR
2008/05/13 Change to 21-41122-02(NSK)
Y6 XTAL 25.000000MHz 12pF ±25PPM 2PIN SMT8.0*4.5*1.4mm NXM25.000AD12F-KAB7-PA NSK LR
U50
XTAL1
XTAL2
(19) GLAN_CLK
R719 RES 33 5% 1/16W SMT0402 LR
JKCLK
(19) LAN_RSTSYNC
JRSTSYNC
(19) LAN_TXD0
(19) LAN_TXD1
(19) LAN_TXD2
JTXD0
JTXD1
JTXD2
(19) LAN_RXD0
(19) LAN_RXD1
(19) LAN_RXD2
JRXD0
JRXD1
JRXD2
LCI
R667 RES 4.87K 1% 1/10W SMT0603 LR
RESET
(18) GLAN_TXP
(18) GLAN_TXN
GLAN_RXP
GLAN_RXN
(18) GLAN_RXP
(18) GLAN_RXN
C820 0.1uF 10V 10% SMT0402 X5R LR
C821 0.1uF 10V 10% SMT0402 X5R LR
GLAN_TXP
GLAN_TXN
GLCI
(40) LAN_MDI0P
(40) LAN_MDI0N
MDI_PLUS_0
MDI_MINUS_0
(40) LAN_MDI1P
(40) LAN_MDI1N
MDI_PLUS_1
MDI_MINUS_1
(40) LAN_MDI2P
(40) LAN_MDI2N
MDI_PLUS_2
MDI_MINUS_2
(40) LAN_MDI3P
(40) LAN_MDI3N
MDI_PLUS_3
MDI_MINUS_3
MDI
RESERVED_NC
R708 10K 5% 1/16W SMT0402 LR
TEST_EN
R678 0 5% 1/16W SMT0402 LR(NU)
IEEE_TEST_N
IEEE_TEST_P
3VDDA_LAN
T38
R713 RES 200 5% 1/16W SMT 0402 LR(NU)
R717 RES 200 5% 1/16W SMT 0402 LR(NU)
R712 RES 200 5% 1/16W SMT 0402 LR(NU)
R707 RES 200 5% 1/16W SMT 0402 LR(NU)
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST
JTCA
ASIC Gigabit PHY 82567LF QFN 56PIN VER:B0 INTEL LR
VCC3_3_1
VCC3_3_2
VCC3_3_3
VCC1_0_1
VCC1_0_2
VCC1_0_3
VCC1_0_4
VCC1_8_1
VCC1_8_2
VCC1_8_3
VCC1_8_4
VCC1_8_5
VCC1_8_6
VCC1_8_7
VCC1_8_8
VCC1_8_9
VCC1_8_10
DIS_REG1_0
CTRL10
CTRL18
LAN_DISABLE_N#
LED0
LED1
LED2
GND_PAD
3VDDA_LAN
+V1.0_LAN_M_IN
2008/05/13 Change to SPWR 0402
SPWR 0 5% 1/16W 0402
R718
+V1.0_LAN_M
+V1.8_LAN_M
DIS_REG1P0
CTRL_10_R
CTRL_18
T47
R680 1K 1% 1/16W SMT0402 LR(NU)
R703 1K 1% 1/16W SMT0402 LR
PM_LAN_ENABLE (20)
LAN_LED_LINK#_ACT
LAN_LED_1000#
LAN_LED_100#
R710 10K 1% 1/16W SMT0402 LR
3VDDA_LAN
L74 SPWR 0 5% 1/16W 0603
R743 4.7K 5% 1/16W SMT0402 LR
C850 0.1uF 16V 80-20% SMT0402 Y5V LR
C847 10uF 6.3V 0603 X5R TAIYO LR
R739 0 5% 1/16W SMT0402 LR
CTRL_18
Q99 TR PNP 2SB1188 -32V -2A MPT3 3PIN ROHM Lead-Free
C839 0.1uF 16V 80-20% SMT0402 Y5V LR
C844 10uF 6.3V 0603 X5R TAIYO LR
+V1.8_LAN
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS
25MIL
C793 10uF 6.3V 0603 X5R TAIYO LR
C789 0.1uF 16V 80-20% SMT0402 Y5V LR
C814 0.1uF 16V 80-20% SMT0402 Y5V LR
C791 0.1uF 16V 80-20% SMT0402 Y5V LR
C802 0.1uF 16V 80-20% SMT0402 Y5V LR
C834 0.1uF 16V 80-20% SMT0402 Y5V LR
V0.3 Modify
DEL
Q97,L72,R727,R728,C840,C841
R650 10K 5% 1/16W SMT0402 LR(NU)
(50,52,53) ADPIN#
Q90 TR NPN DTC144EUAT106 50V 100mA UMT3(SC-70) 3PIN ROHM LR(NU)
D51 DIODE SWITCHING PS355NS 80V 100mA SMT0805 2PIN PSI LR(NU)
(50,54) LAN_DIS
D52 DIODE SWITCHING PS355NS 80V 100mA SMT0805 2PIN PSI LR
Q96 TRANS M-FET-P APM2301AAC-TRL -20V -3A SOT23 3PIN ANPEC LR
R656 100K 5% 1/16W SMT0402 LR
C781 0.1uF 10V 10% SMT0402 X5R LR
R655 10K 5% 1/16W SMT0402 LR
R654 0 5% 1/16W SMT0402 LR(NU)
Q94 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS
25MIL
C817 0.1uF 16V 80-20% SMT0402 Y5V LR
C827 10uF 6.3V 0603 X5R TAIYO LR
C851 4.7uF 10V +80-20% 0805 Y5V LR
C848 0.1uF 16V 80-20% SMT0402 Y5V LR
C832 0.1uF 16V 80-20% SMT0402 Y5V LR
C803 0.1uF 16V 80-20% SMT0402 Y5V LR
C811 4.7uF 10V +80-20% 0805 Y5V LR
C815 4.7uF 10V +80-20% 0805 Y5V LR
+V1.0_LAN_M_IN
3VDDA_LAN
+V1.8_LAN_M
3VDDA
(8,18,20,21,22,24,32,37,38,41,45,47,48,49,50,52,54,55,58)
V0.3 EMI Modify 0613
600 ±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR
L79
C986 0.1uF 16V 80-20% SMT0402 Y5V LR
C822 0.1uF 16V 80-20% SMT0402 Y5V LR
R735 0 5% 1/10W SMT0603 LR
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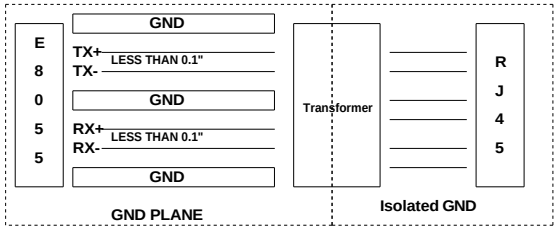
TX
RX

100 ohm ---> trace 4 mil , space 10 mil
50 mil space from other signals
Total Tace Length no more thans 4.8"
2 Differential pairs must have the same length



(39) +V1.8_LAN_M

L71
0 5% 1/10W SMT0603 LR

R665
0 5% 1/16W SMT0402 LR

U47

(39) LAN_MDI0P
(39) LAN_MDI0N
(39) LAN_MDI1P
(39) LAN_MDI1N
(39) LAN_MDI2P
(39) LAN_MDI2N
(39) LAN_MDI3P
(39) LAN_MDI3N

1	TCT1	MCT1	24
2	TD1+	MX1+	23
3	TD1-	MX1-	22
4	TCT2	MCT2	21
5	TD2+	MX2+	20
6	TD2-	MX2-	19
7	TCT3	MCT3	18
8	TD3+	MX3+	17
9	TD3-	MX3-	16
10	TCT4	MCT4	15
11	TD4+	MX4+	14
12	TD4-	MX4-	13

R642 75 1% 1/16W SMT0402 LR — LAN_TXD0+
R643 75 1% 1/16W SMT0402 LR — LAN_TXD0-
R644 75 1% 1/16W SMT0402 LR — LAN_TXD1+
R645 75 1% 1/16W SMT0402 LR — LAN_TXD1-
LAN_TXD2+
LAN_TXD2-
LAN_TXD3+
LAN_TXD3-

TRANSFOMER 350uH 0.1V 8mA 24PIN HPL-5001-3 HWS LR

C761
1500pF 2KV ±10% SMT1206 X7R 1206B152K202LT WALSIN LR

L_GND

PLACE RC NETWORKS CLOSE TO P HY CHIP

R654 R663 R662 R661 R660 R659 R658 R657
49.9 1% 1/16W SMT0402 LR(NU)
Rc Rc Rc Rc

C786 C785 C784 C783
0.01uF 16V 10% SMT0402 X7R LR(NU)

C780 C779
0.1uF 16V 80-20% SMT0402 Y5V LR

V0.2 Modify for BOM

	for Giga LAN	for 10/100 LAN
Rc	STUFF	NU
La	STUFF	NU

LAN_L_TXD0+ C923 MO-CAP 5pF 50V ±0.5pF SMT0402 NPO LR(NU)
LAN_L_TXD0- C924 MO-CAP 5pF 50V ±0.5pF SMT0402 NPO LR(NU)
LAN_L_TXD1+ C925 MO-CAP 5pF 50V ±0.5pF SMT0402 NPO LR(NU)
LAN_L_TXD1- C926 MO-CAP 5pF 50V ±0.5pF SMT0402 NPO LR(NU)
LAN_L_TXD2+ C927 MO-CAP 5pF 50V ±0.5pF SMT0402 NPO LR(NU)
LAN_L_TXD2- C928 MO-CAP 5pF 50V ±0.5pF SMT0402 NPO LR(NU)
LAN_L_TXD3+ C929 MO-CAP 5pF 50V ±0.5pF SMT0402 NPO LR(NU)
LAN_L_TXD3- C930 MO-CAP 5pF 50V ±0.5pF SMT0402 NPO LR(NU)
L_GND
For EMI

These 3 capacitor s across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.

C452
0.1uF 16V 80-20% SMT0603 Y5V LR(NU)
L_GND

L69
L68
La

LAN_TXD1+	1	8	LAN_L_TXD1+
LAN_TXD1-	2	7	LAN_L_TXD1-
LAN_TXD0-	3	6	LAN_L_TXD0-
LAN_TXD0+	4	5	LAN_L_TXD0+
LAN_TXD3-	1	8	LAN_L_TXD3-
LAN_TXD3+	2	7	LAN_L_TXD3+
LAN_TXD2-	3	6	LAN_L_TXD2-
LAN_TXD2+	4	5	LAN_L_TXD2+

COMMON-MODE CHOKE 180 25% 100MHz 400mA SMT1012 8PIN YCM1012V4SF-181T04 YOSONIC LR
COMMON-MODE CHOKE 180 25% 100MHz 400mA SMT1012 8PIN YCM1012V4SF-181T04 YOSONIC LR

CN31
LAN_L_TXD0+
LAN_L_TXD0-
LAN_L_TXD1+
LAN_L_TXD1-
LAN_L_TXD2+
LAN_L_TXD2-
LAN_L_TXD3+
LAN_L_TXD3-
L_GND
R354 0 5% 1/10W SMT0603 LR
20-25351-00
CON Alltop C10001-108A4-L SMD RJ45 8Pin P=1.0 Deep H=8.6 LR

(39) +V1.8_LAN_M +V1.8_LAN_M

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Size: C
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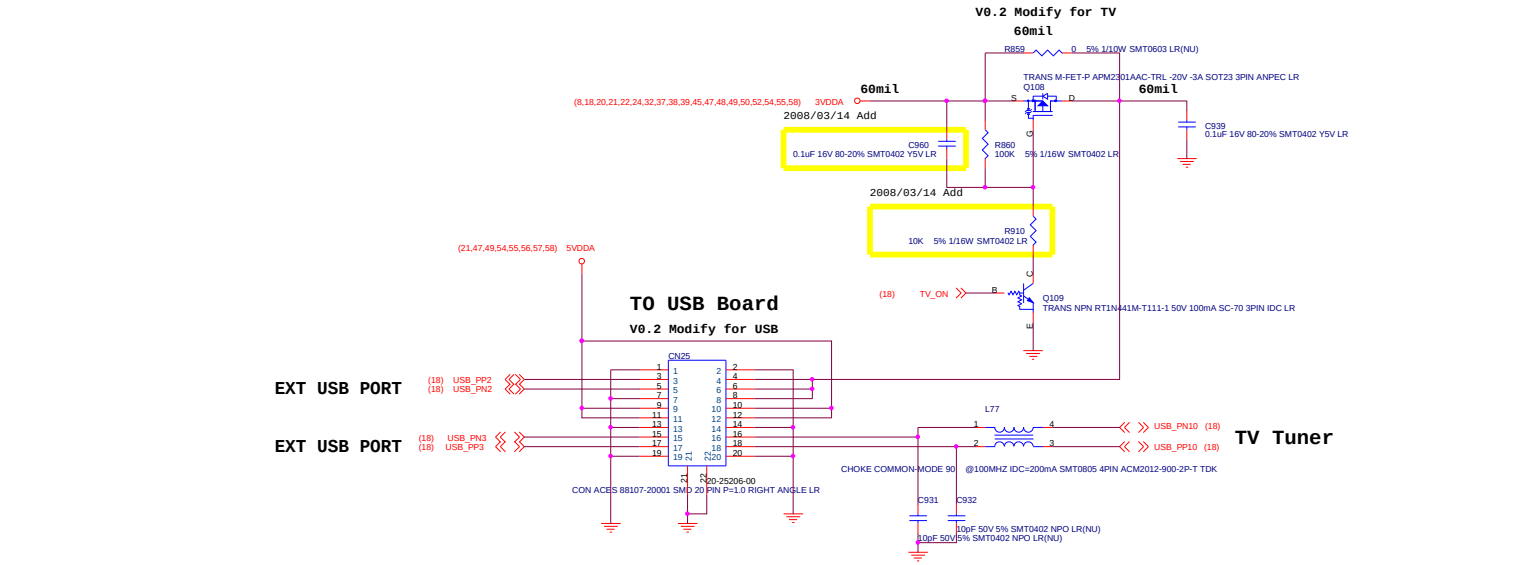

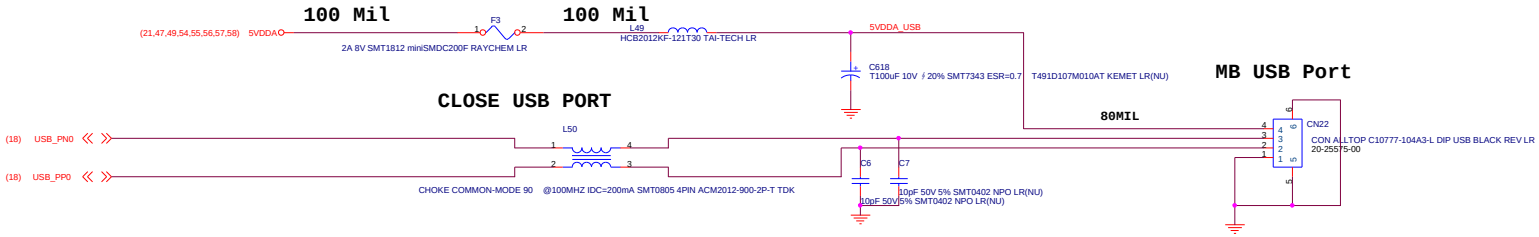

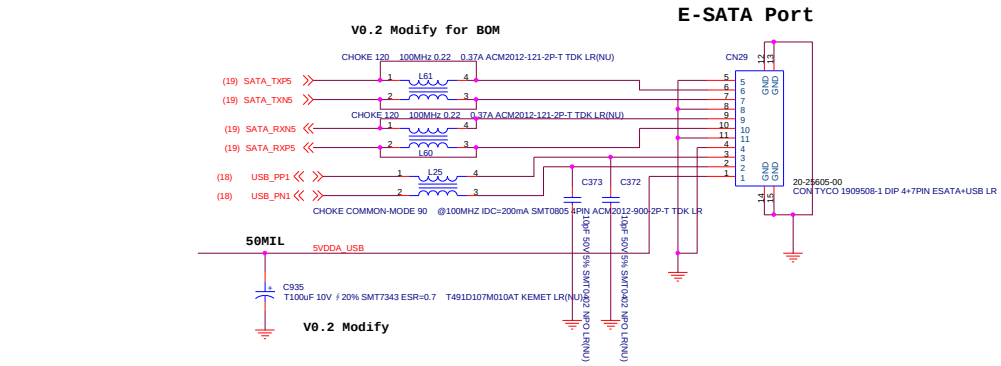

(21,47,49,54,55,56,57,58) 5VDDA 5VDDA

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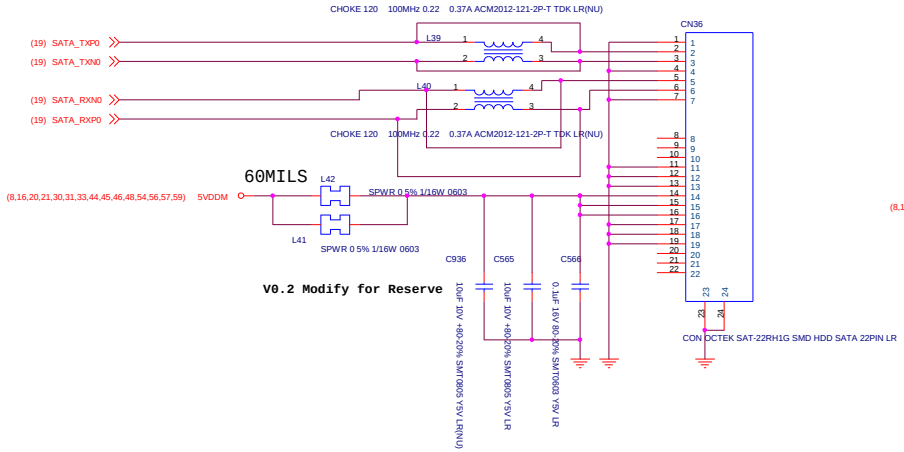
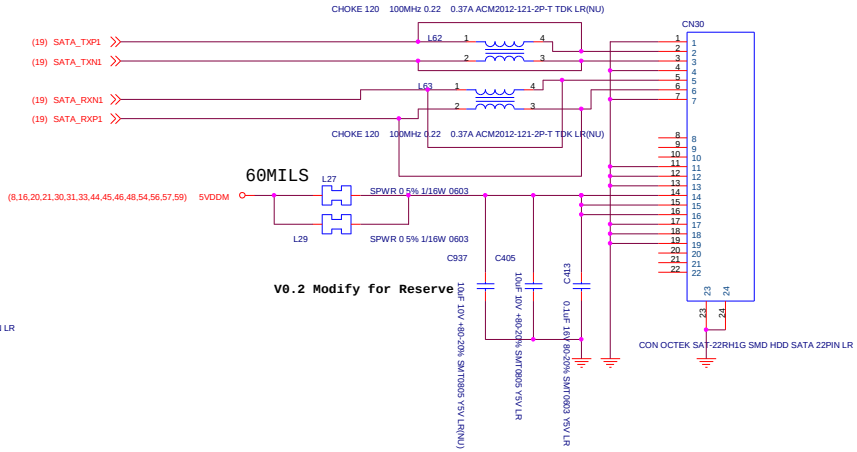
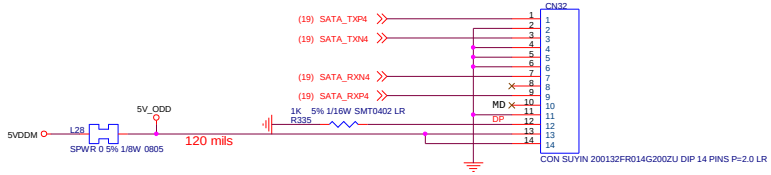
HDD I/F





2008_05_04 Modify

SATA ODD CN



(8,16,20,21,30,31,33,44,45,46,48,54,56,57,59) 5VDDM 5VDDM

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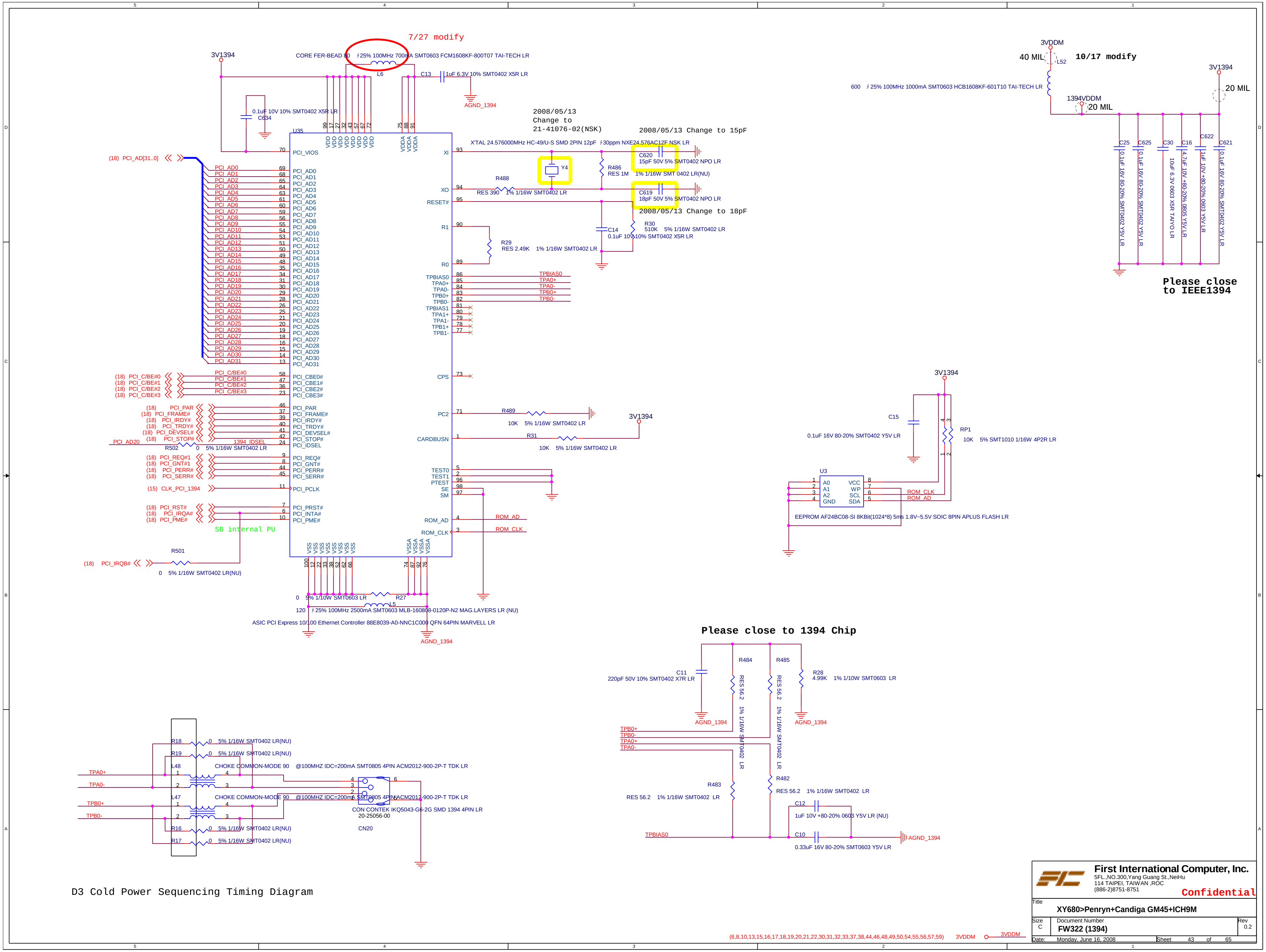
7/27 modify
3V1394
CORE FER-BEAD 80 25% 100MHz 700mA SMT0603 FCM1608KF-800T07 TAI-TECH LR
L6
C13 1uF 6.3V 10% SMT0402 X5R LR
AGND_1394
0.1uF 10V 10% SMT0402 X5R LR
C634
U35
2008/05/13
Change to
21-41076-02(NSK)
2008/05/13 Change to 15pF
X'TAL 24.576000MHz HC-49/U-S SMD 2PIN 12pF 30ppm NXE24.576AC12F NSK LR
C620 15pF 50V 5% SMT0402 NPO LR
R486 RES 1M 1% 1/16W SMT 0402 LR(NU)
Y4
R488
RES 390 1% 1/16W SMT0402 LR
C619 18pF 50V 5% SMT0402 NPO LR
2008/05/13 Change to 18pF
R30 510K 5% 1/16W SMT0402 LR
C14 0.1uF 10V 10% SMT0402 X5R LR
R29 RES 2.49K 1% 1/16W SMT0402 LR
(18) PCI_AD[31..0]
PCI_VIOS
XI
XO
RESET#
R1
R0
TPBIAS0 TPA0+ TPA0- TPB0+ TPB0- TPBIAS1 TPA1+ TPA1- TPB1+ TPB1-
CPS
PC2
CARDBUSN
TEST0 TEST1 PTEST SE SM
ROM_AD
ROM_CLK
PCI_AD0 … PCI_AD31
(18) PCI_C/BE#0
(18) PCI_C/BE#1
(18) PCI_C/BE#2
(18) PCI_C/BE#3
(18) PCI_PAR
(18) PCI_FRAME#
(18) PCI_IRDY#
(18) PCI_TRDY#
(18) PCI_DEVSEL#
(18) PCI_STOP#
PCI_AD20 1394_IDSEL
R502 0 5% 1/16W SMT0402 LR
(18) PCI_REQ#1
(18) PCI_GNT#1
(18) PCI_PERR#
(18) PCI_SERR#
(15) CLK_PCI_1394
(18) PCI_RST#
(18) PCI_IRQA#
(18) PCI_PME#
SB internal PU
R501
(18) PCI_IRQB#
0 5% 1/16W SMT0402 LR(NU)
R489 10K 5% 1/16W SMT0402 LR
3V1394
R31 10K 5% 1/16W SMT0402 LR
0 5% 1/10W SMT0603 LR R27
120 25% 100MHz 2500mA SMT0603 MLB-160808-0120P-N2 MAG.LAYERS LR (NU) L5
ASIC PCI Express 10/100 Ethernet Controller 88E8039-A0-NNC1C000 QFN 64PIN MARVELL LR
AGND_1394
3VDDM
40 MIL L52
10/17 modify
600 25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR
1394VDDM 20 MIL
3V1394 20 MIL
C25 0.1uF 16V 80-20% SMT0402 Y5V LR
C625 0.1uF 16V 80-20% SMT0402 Y5V LR
C30 10uF 6.3V 0603 X5R TAIYO LR
C16 4.7uF 10V +80-20% 0805 Y5V LR
C622 1uF 10V +80-20% 0603 Y5V LR
C621 0.1uF 16V 80-20% SMT0402 Y5V LR
Please close to IEEE1394
3V1394
C15 0.1uF 16V 80-20% SMT0402 Y5V LR
RP1 10K 5% SMT1010 1/16W 4P2R LR
U3 A0 A1 A2 GND VCC WP SCL SDA
ROM_CLK
ROM_AD
EEPROM AF24BC08-SI 8KBit(1024*8) 5ms 1.8V~5.5V SOIC 8PIN APLUS FLASH LR
Please close to 1394 Chip
C11 220pF 50V 10% SMT0402 X7R LR
R484 RES 56.2 1% 1/16W SMT0402 LR
R485 RES 56.2 1% 1/16W SMT0402 LR
R28 4.99K 1% 1/10W SMT0603 LR
AGND_1394
TPB0+ TPB0- TPA0+ TPA0-
R483 RES 56.2 1% 1/16W SMT0402 LR
R482 RES 56.2 1% 1/16W SMT0402 LR
C12 1uF 10V +80-20% 0603 Y5V LR (NU)
TPBIAS0
C10 0.33uF 16V 80-20% SMT0603 Y5V LR
AGND_1394
R18 0 5% 1/16W SMT0402 LR(NU)
R19 0 5% 1/16W SMT0402 LR(NU)
L48 CHOKE COMMON-MODE 90 @100MHZ IDC=200mA SMT0805 4PIN ACM2012-900-2P-T TDK LR
TPA0+ TPA0-
TPB0+ TPB0-
L47 CHOKE COMMON-MODE 90 @100MHZ IDC=200mA SMT0805 4PIN ACM2012-900-2P-T TDK LR
CON CONTEK IKQ5043-G6-2G SMD 1394 4PIN LR
20-25056-00
CN20
R16 0 5% 1/16W SMT0402 LR(NU)
R17 0 5% 1/16W SMT0402 LR(NU)
D3 Cold Power Sequencing Timing Diagram
(6,8,10,13,15,16,17,18,19,20,21,22,30,31,32,33,37,38,44,46,48,49,50,54,55,56,57,59) 3VDDM 3VDDM
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Title
XY680>Penryn+Candiga GM45+ICH9M
Size C
Document Number FW322 (1394)
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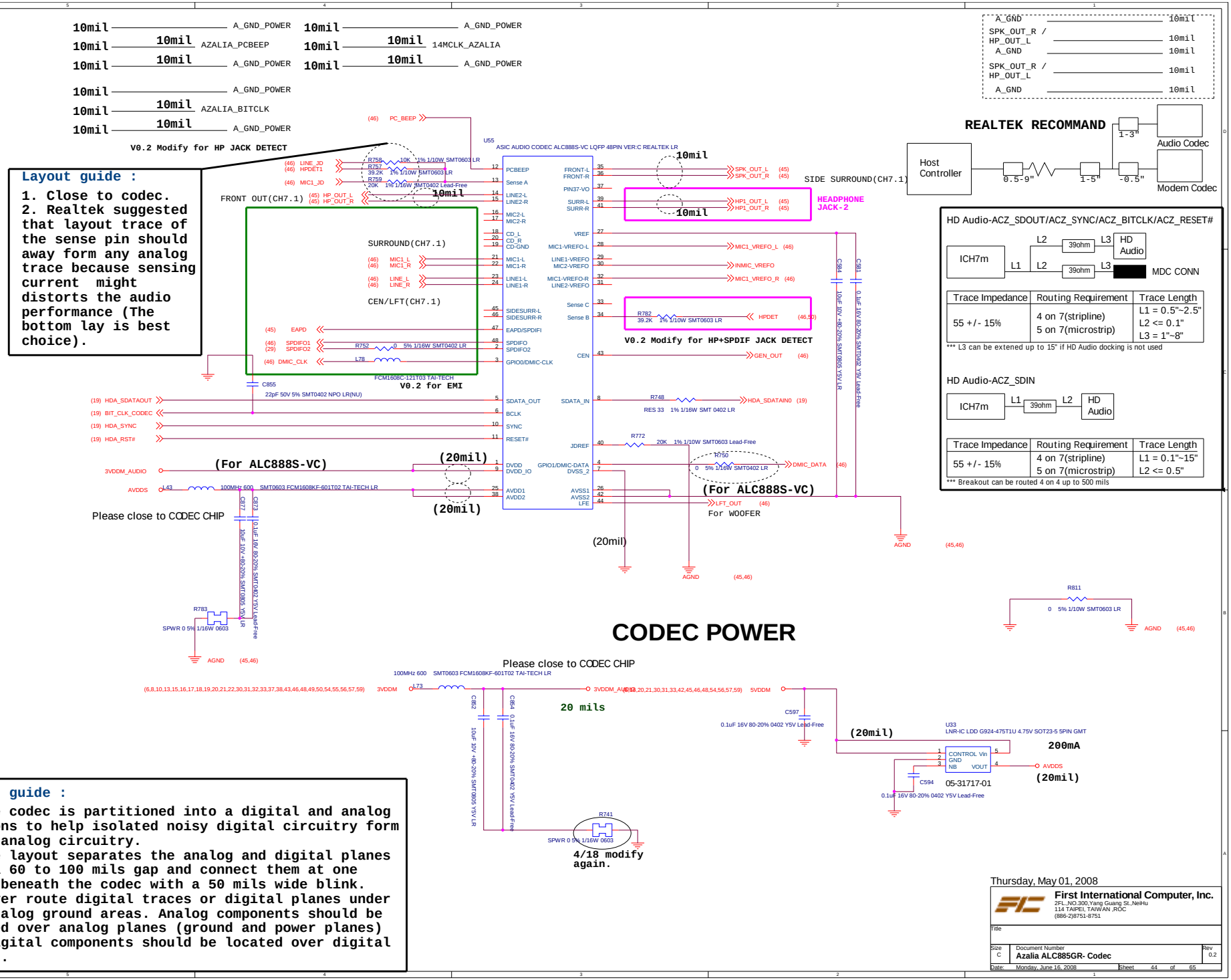
10mil A_GND_POWER
10mil AZALIA_PCBEEP
10mil A_GND_POWER
10mil A_GND_POWER
10mil 14MCLK_AZALIA
10mil A_GND_POWER
10mil A_GND_POWER
10mil AZALIA_BITCLK
10mil A_GND_POWER
V0.2 Modify for HP JACK DETECT
Layout guide :
1. Close to codec.
2. Realtek suggested that layout trace of the sense pin should away form any analog trace because sensing current might distorts the audio performance (The bottom lay is best choice).
A_GND 10mil
SPK_OUT_R / HP_OUT_L 10mil
A_GND 10mil
SPK_OUT_R / HP_OUT_L 10mil
A_GND 10mil
REALTEK RECOMMAND
Host Controller
0.5-9"
1-5"
1-3"
-0.5"
Audio Codec
Modem Codec
U55
ASIC AUDIO CODEC ALC888S-VC LQFP 48PIN VER:C REALTEK LR
FRONT OUT(CH7.1)
SURROUND(CH7.1)
CEN/LFT(CH7.1)
SIDE SURROUND(CH7.1)
HEADPHONE JACK-2
V0.2 Modify for HP+SPDIF JACK DETECT
V0.2 for EMI
FCM1608C-121T03 TAI-TECH
(For ALC888S-VC)
(For ALC888S-VC)
For WOOFER
Please close to CODEC CHIP
(20mil)
HD Audio-ACZ_SDOUT/ACZ_SYNC/ACZ_BITCLK/ACZ_RESET#
ICH7m
HD Audio
MDC CONN
39ohm
Trace Impedance | Routing Requirement | Trace Length
55 +/- 15% | 4 on 7(stripline) 5 on 7(microstrip) | L1 = 0.5"~2.5" L2 <= 0.1" L3 = 1"~8"
*** L3 can be extened up to 15" if HD Audio docking is not used
HD Audio-ACZ_SDIN
ICH7m
39ohm
HD Audio
Trace Impedance | Routing Requirement | Trace Length
55 +/- 15% | 4 on 7(stripline) 5 on 7(microstrip) | L1 = 0.1"~15" L2 <= 0.5"
*** Breakout can be routed 4 on 4 up to 500 mils
CODEC POWER
Please close to CODEC CHIP
100MHz 600 SMT0603 FCM1608KF-601T02 TAI-TECH LR
20 mils
(20mil)
U33
LNR-IC LDD G924-475T1U 4.75V SOT23-5 5PIN GMT
200mA
05-31717-01
4/18 modify again.
Layout guide :
1. The codec is partitioned into a digital and analog sections to help isolated noisy digital circuitry form quiet analog circuitry.
2. The layout separates the analog and digital planes with a 60 to 100 mils gap and connect them at one point beneath the codec with a 50 mils wide blink.
3. Never route digital traces or digital planes under the analog ground areas. Analog components should be located over analog planes (ground and power planes) and digital components should be located over digital planes.
Thursday, May 01, 2008
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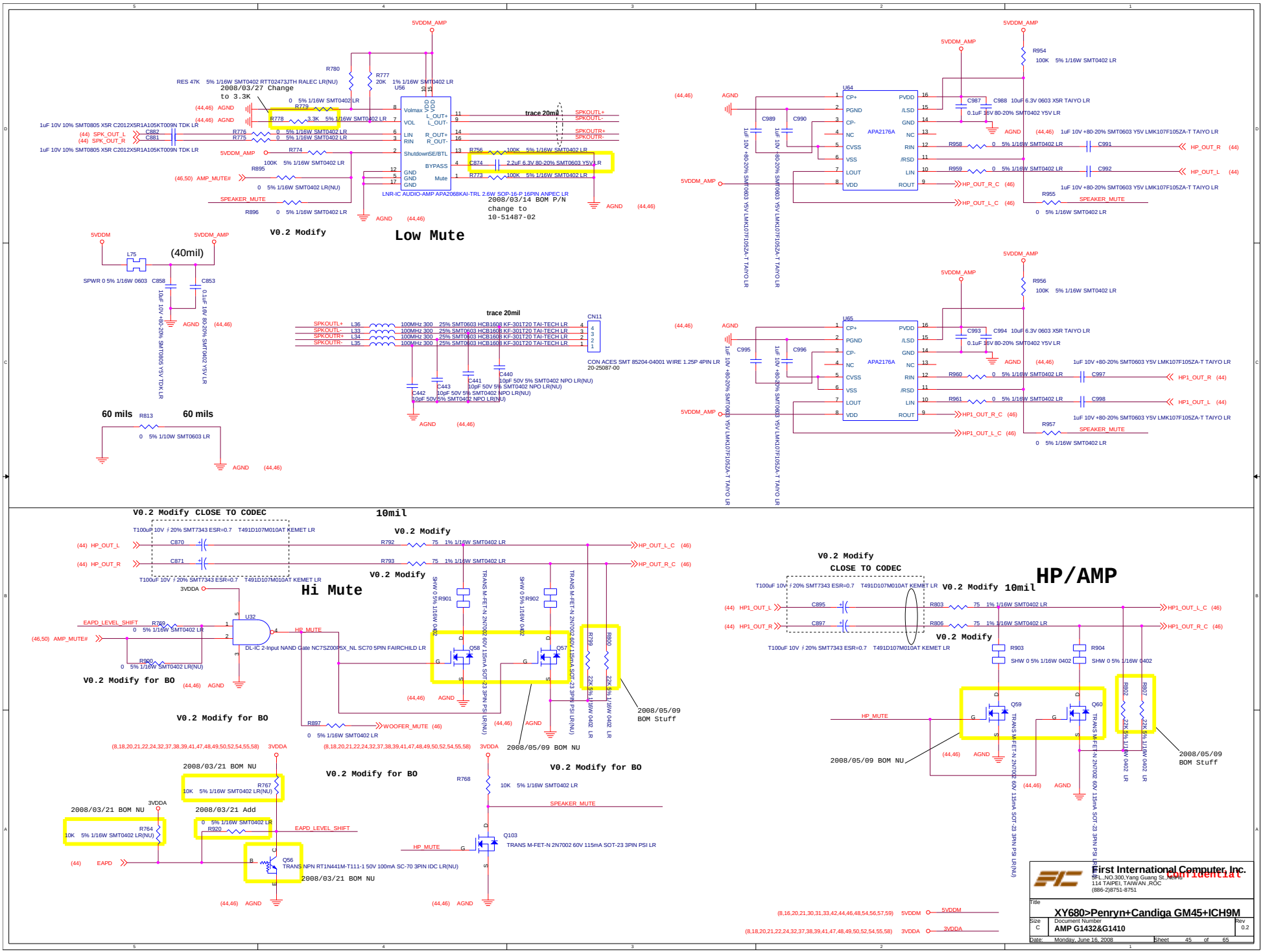
(886-2)8751-8751
Title
Size C
Document Number Azalia ALC885GR- Codec
Rev 0.2
Date: Monday, June 16, 2008
Sheet 44 of 65


Low Mute
HP/AMP
Hi Mute
V0.2 Modify
V0.2 Modify for BO
2008/03/27 Change to 3.3K
2008/03/14 BOM P/N change to 10-51487-02
2008/05/09 BOM Stuff
2008/05/09 BOM NU
2008/03/21 BOM NU
2008/03/21 Add
trace 20mil
10mil
60 mils
(40mil)
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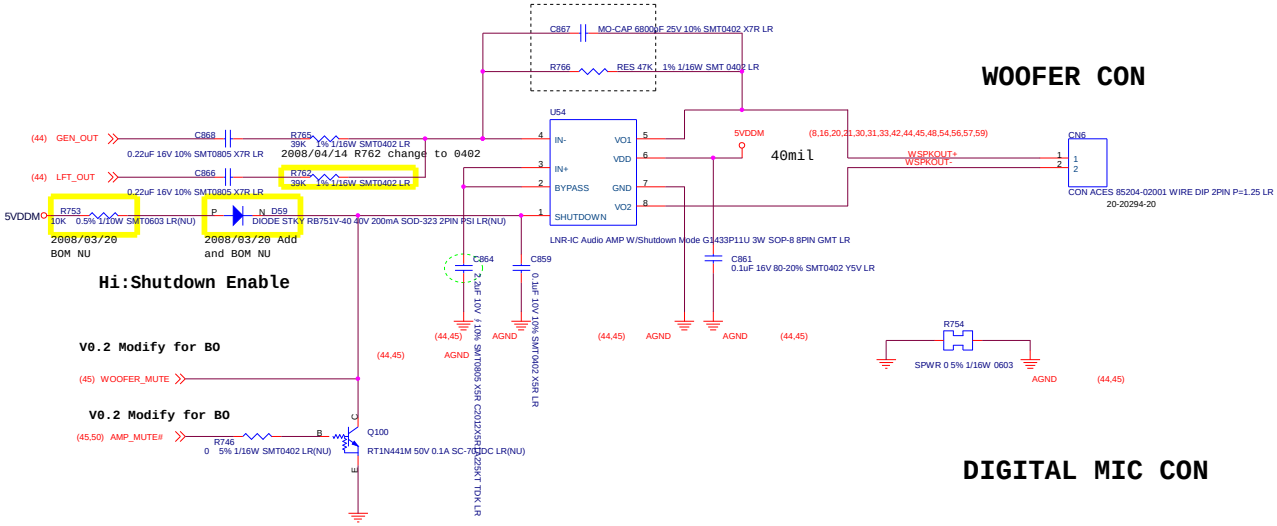
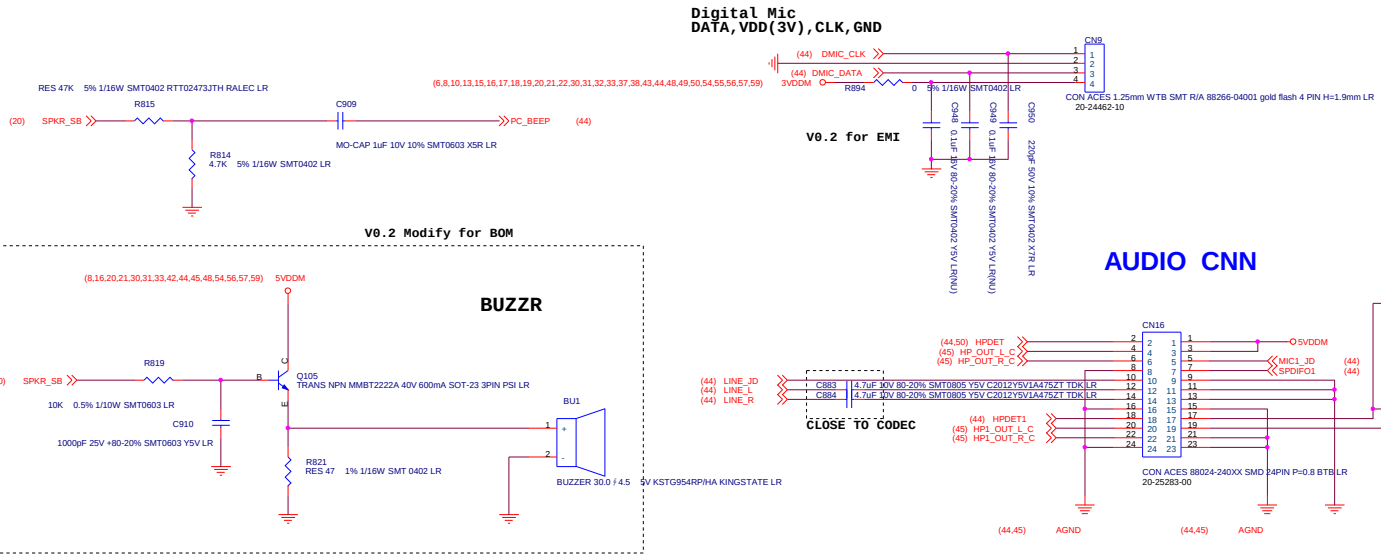
Confidential
XY680>Penryn+Candiga GM45+ICH9M
AMP G1432&G1410
Monday, June 16, 2008

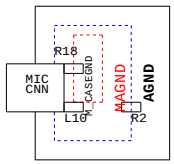
SUB-WOOFER

fo = 1/ 2*piRC ... (R319*C524)

Gain = Rf/Ri ... (R319/R60)







(8,16,20,21,30,31,33,42,44,45,48,54,56,57,59) 5VDDM 5VDDM

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Size C	Document Number HP OUT / MIC IN / LINE IN	Rev 0.2
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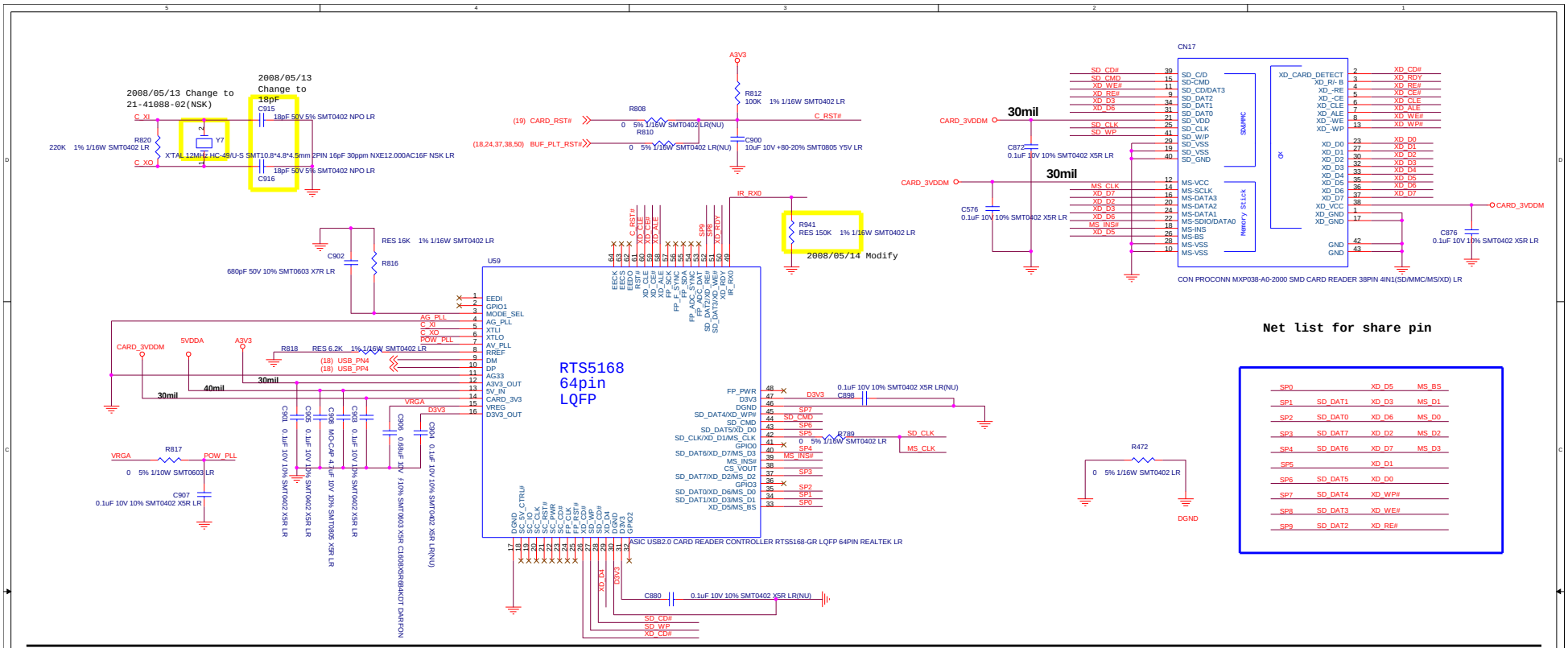

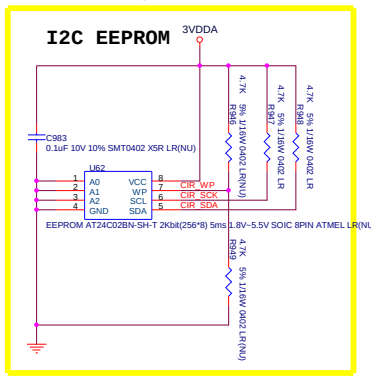

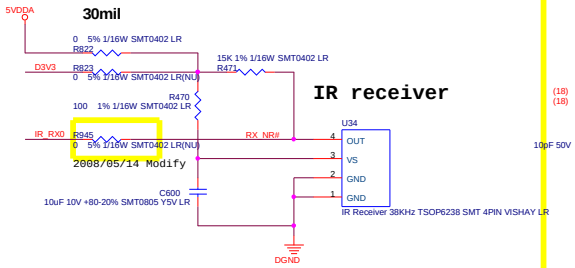

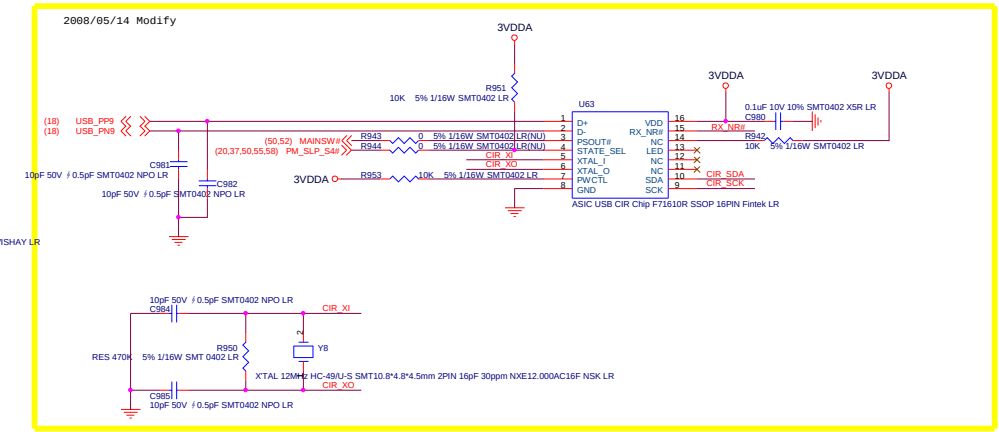

(8,18,20,21,22,24,32,37,38,39,41,45,48,49,50,52,54,55,58) 3VDDA 3VDDA
(21,41,49,54,55,56,57,58) 5VDDA 5VDDA

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Title: XY680>Penryn+Candiga GM45+ICH9M
Size: C | Document Number: Cardreader RTS5168 | Rev: 0.2
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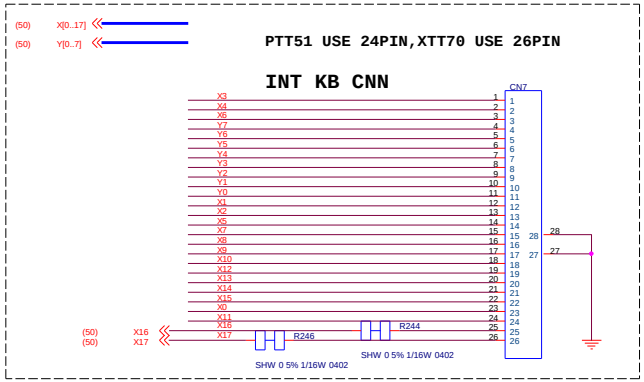
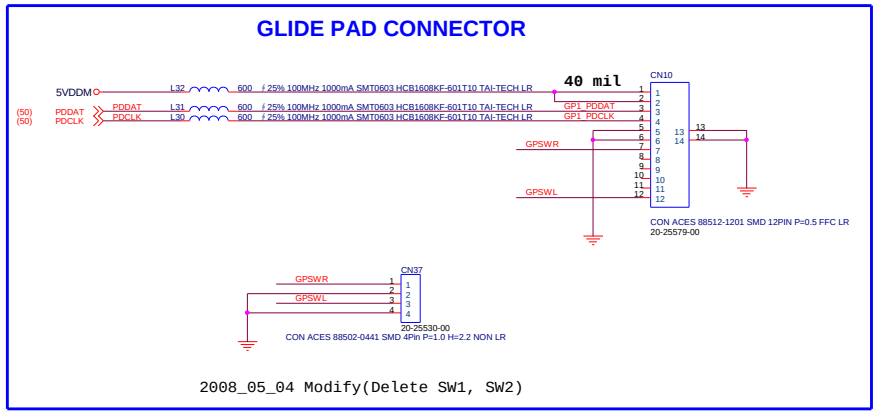
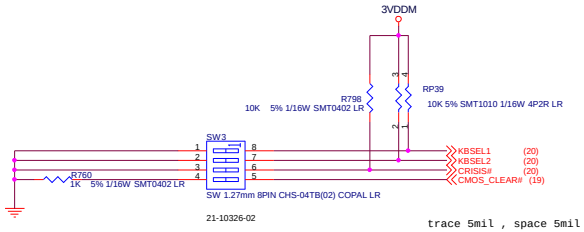


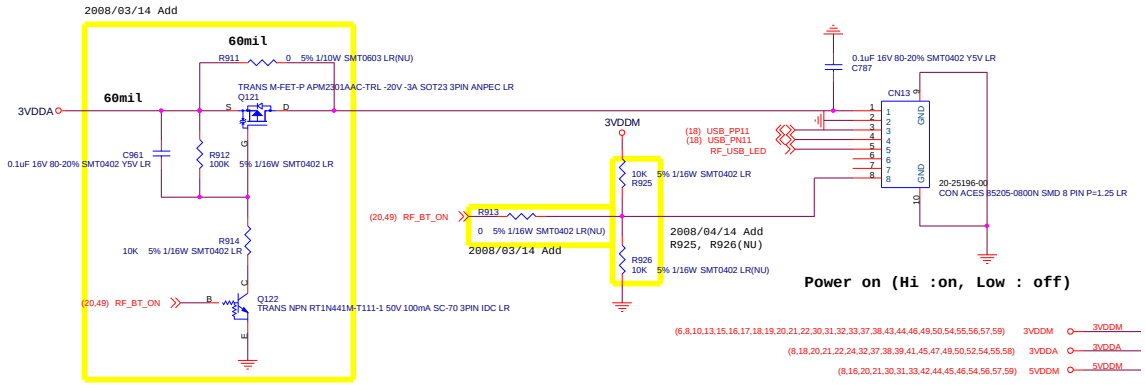


DIP SWITCH



KBSEL2	KBSEL1	
ON	ON	UK Keyboard
	OFF	Reserved
OFF		JP Keyboard
OFF	OFF	US Keyboard

CRISIS#	ON	CRISIS mode
	OFF	Normal
CMOS_CLEAR#	ON	Reset RTC
	OFF	NONE



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Size: C | Document Number: <INT K/B /GP/SW CNN> | Rev: 0.2

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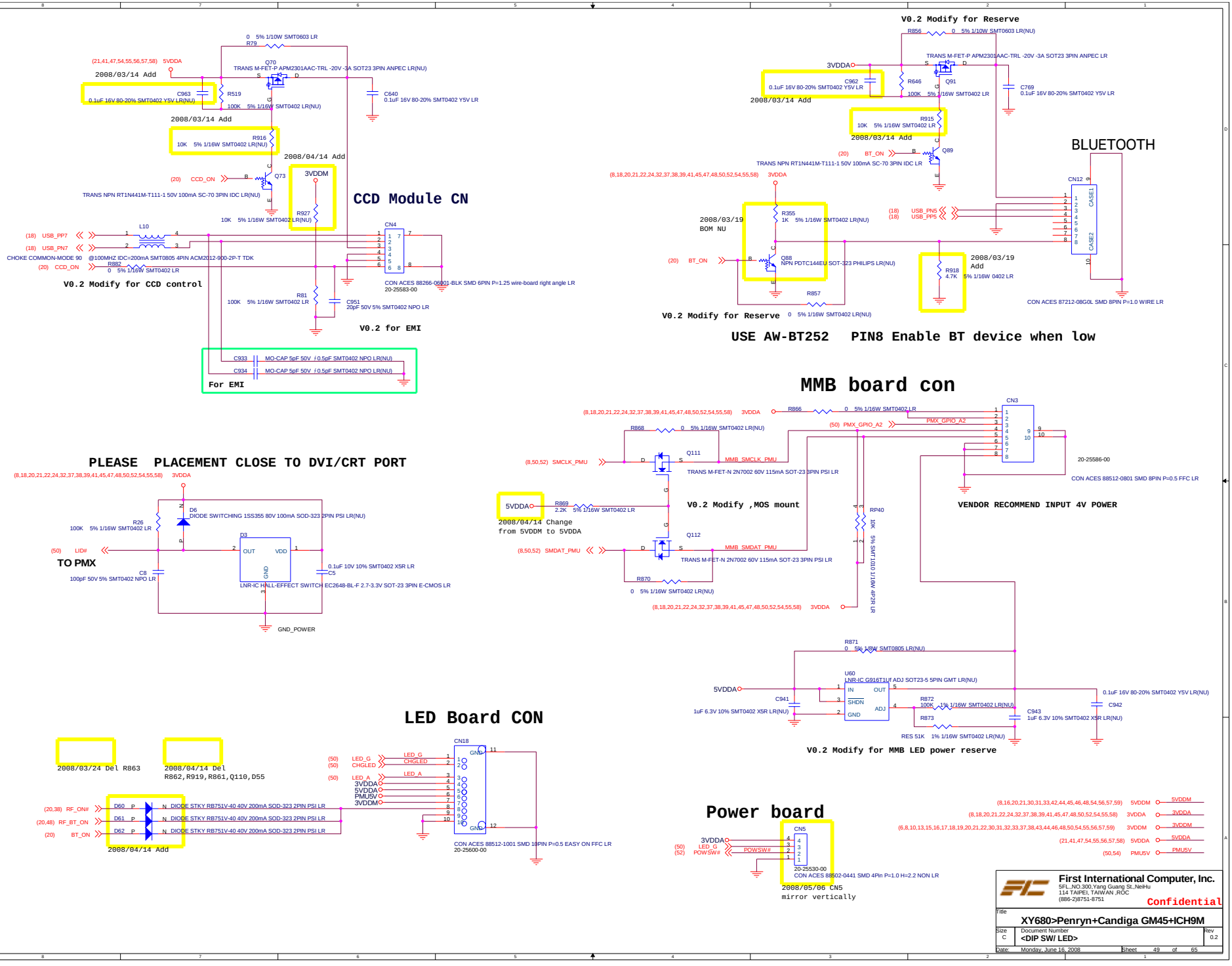
CCD Module CN
V0.2 Modify for CCD control
V0.2 for EMI
For EMI
V0.2 Modify for Reserve
BLUETOOTH
USE AW-BT252 PIN8 Enable BT device when low
MMB board con
PLEASE PLACEMENT CLOSE TO DVI/CRT PORT
TO PMX
V0.2 Modify ,MOS mount
VENDOR RECOMMEND INPUT 4V POWER
LED Board CON
V0.2 Modify for MMB LED power reserve
Power board
2008/05/06 CN5
mirror vertically
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XY680>Penryn+Candiga GM45+ICH9M
<DIP SW/ LED>

SYSTEM POWER OVP

PMX

BOM is 05-23690-05

2008/05/12
BOM NU

2008/05/07 Add

2008/05/13
Change to
21-41129-02(NSK)

V0.2 Modify

2008/05/14 Add

2008/04/14 Add

2008/03/14 Modify

V0.2 Modify for Power

V0.2 Modify for MMB

chipset platform ID

REF33

BATTERY VOLTAGE SENSE

20060322A

Close to PMX

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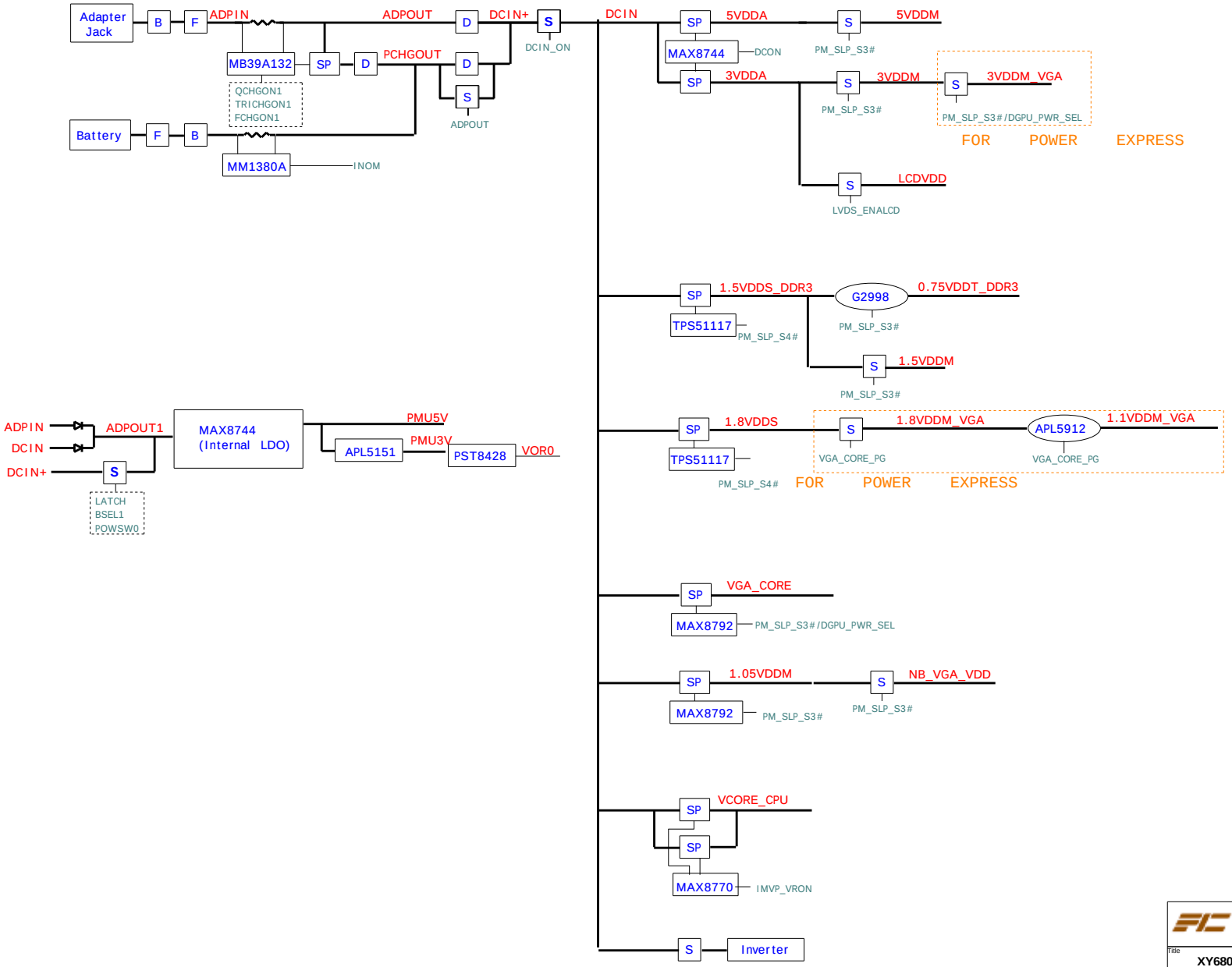
XY670 Power Block



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Size: C | Document Number: Power Block | Rev: 0.2

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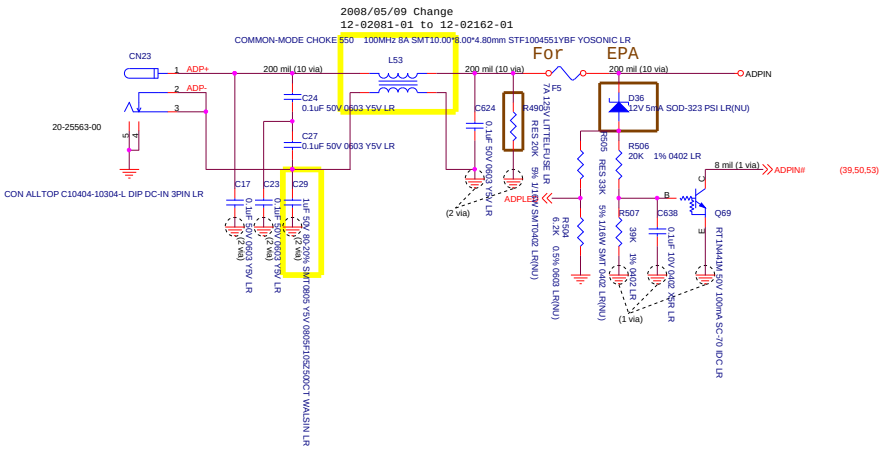
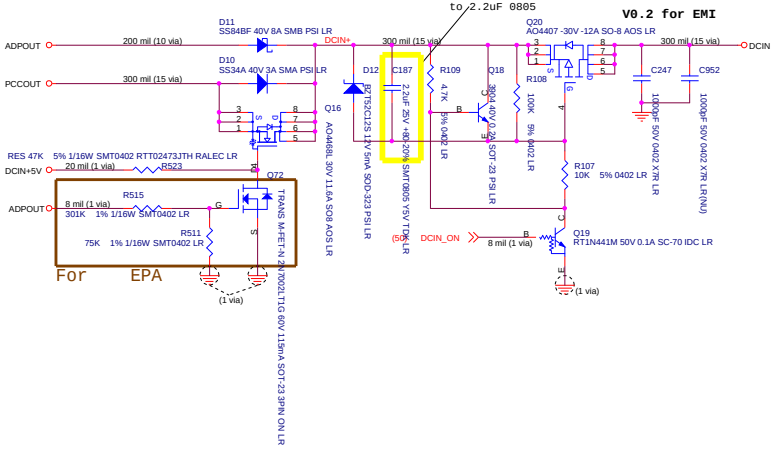
ADPIN, PCCOUT, DCIN, ADPOUT+

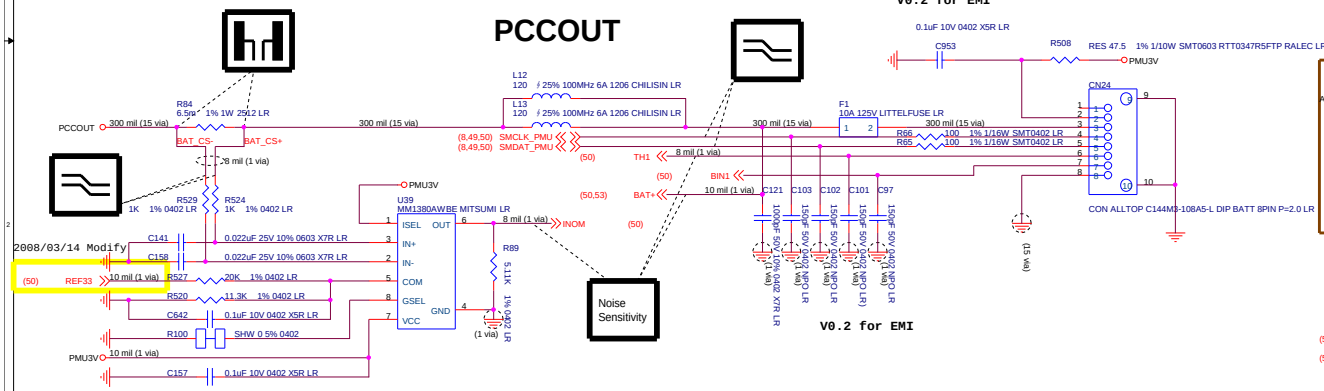
ADPIN



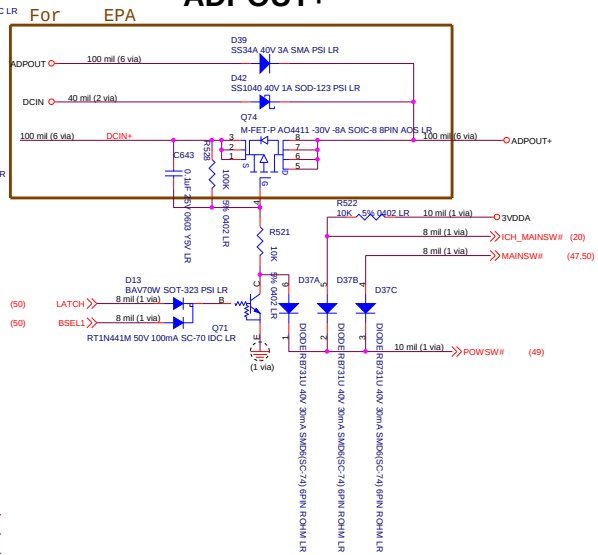
DCIN



PCCOUT



ADPOUT+



(53) ADPIN — ADPIN
(53) ADPOUT — ADPOUT
(53) PCCOUT — PCCOUT
(54) DCIN+5V — DCIN+5V
(32,54,55,56,57,58,59) DCIN — DCIN
(19,50,54) PMU3V — PMU3V
(54) ADPOUT+ — ADPOUT+
(8,18,20,21,22,24,32,37,38,39,41,45,47,48,49,50,54,55,58) 3VDDA — 3VDDA

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Size: C | Document Number: ACIN / DCIN | Rev: 0.2
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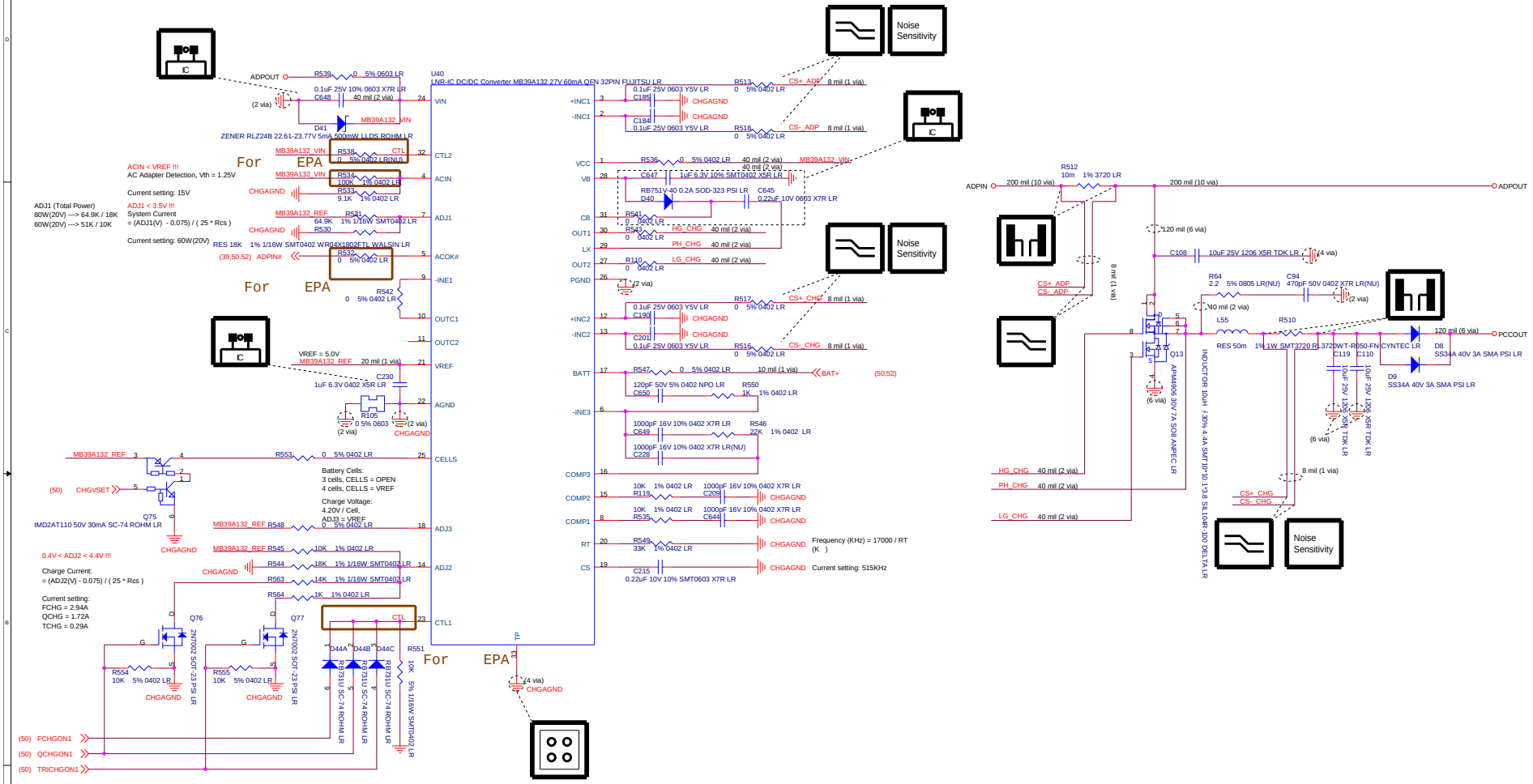
Charger



(52) ADPIN — ADPIN
(52) ADPOUT — ADPOUT
(52) PCCOUT — PCCOUT

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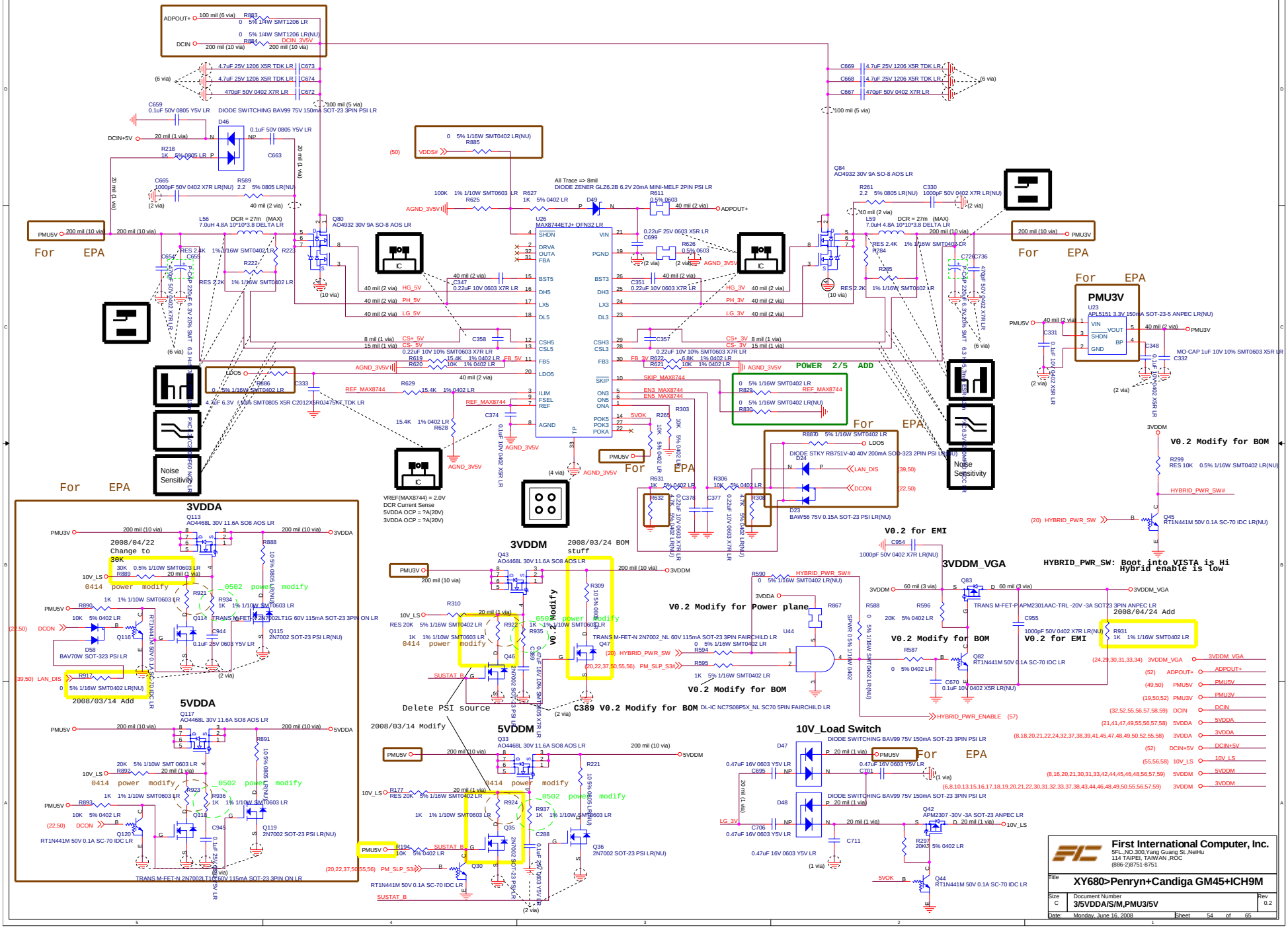
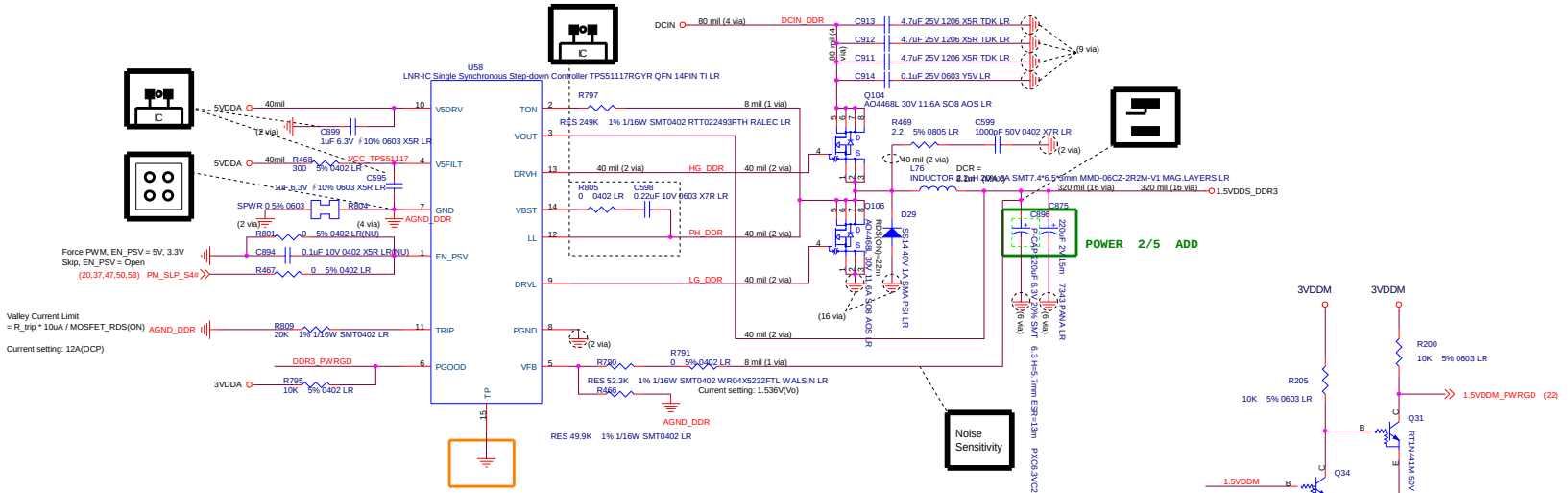
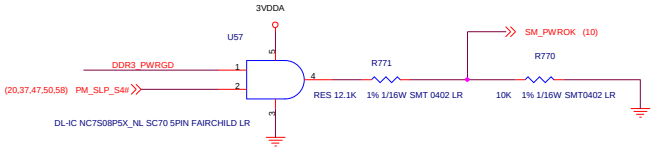
PMU5V, PMU3V, 5VDDA/S/M, 3VDDA/S/M, 1.5VDDA



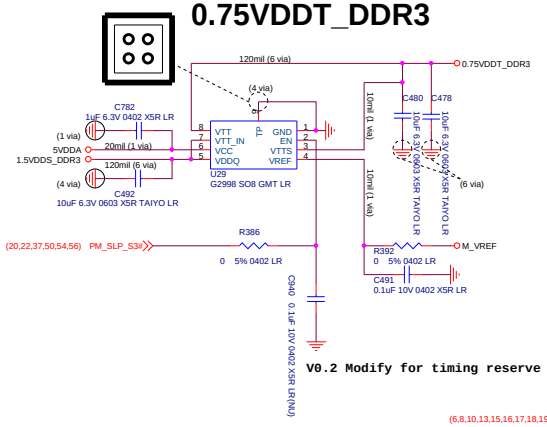
DDR 1.5VDDS/M, 0.75VDDS

DDR1.5VDDS



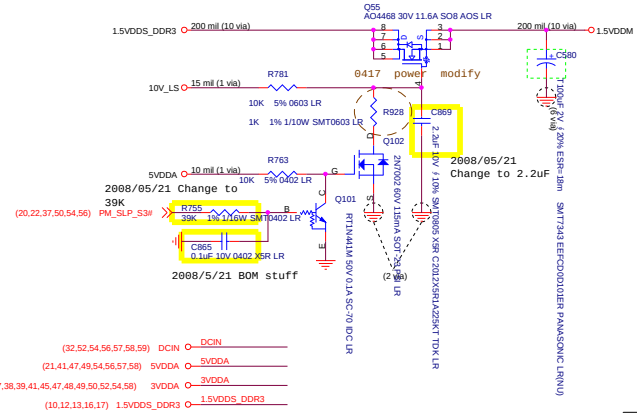


0.75VDDT_DDR3



V0.2 Modify for timing reserve

1.5VDDM



(32,52,54,56,57,58,59) DCIN
(21,41,47,49,54,56,57,58) 5VDDA
(8,18,20,21,22,24,32,37,38,39,41,45,47,48,49,50,52,54,58) 3VDDA
(10,12,13,16,17) 1.5VDDS_DDR3
(16,17) 0.75VDDT_DDR3
(10,16,17) M_VREF
(54,56,58) 10V_LS
(7,12,13,18,19,21,37,38) 1.5VDDM
(6,8,10,13,15,16,17,18,19,20,21,22,30,31,32,33,37,38,43,44,46,48,49,50,54,56,57,59) 3VDDM

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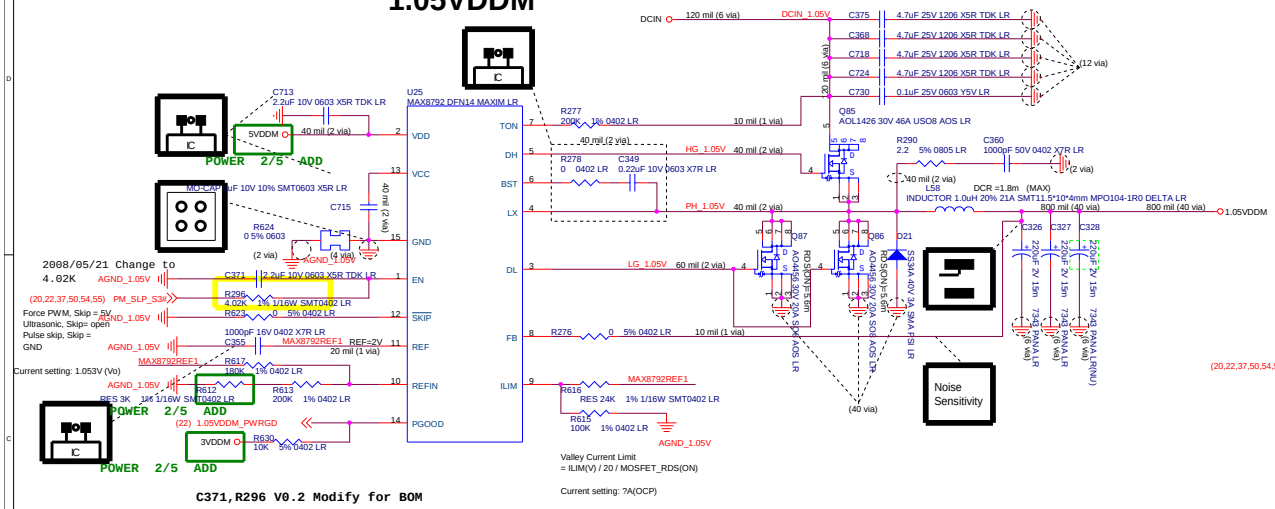
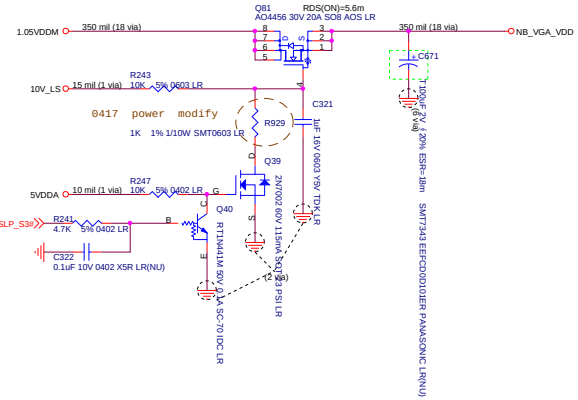
Cantiga 1.05VDDM

1.05VDDM



FOR NB TIMING CREATE POWER PLANE

Cantiga_VGA_VDD



(21,41,47,49,54,55,57,58) 5VDDA — 5VDDA

(32,52,54,55,57,58,59) DCIN — DCIN

(8,16,20,21,30,31,33,42,44,45,46,48,54,57,59) 5VDDM — 5VDDM

(6,8,10,13,15,16,17,18,19,20,21,22,30,31,32,33,37,38,43,44,46,48,49,50,54,55,57,59) 3VDDM — 3VDDM

POWER 2/5 ADD

(6,7,9,10,12,13,15,19,21) 1.05VDDM — 1.05VDDM

(54,55,58) 10V_LS — 10V_LS

(12) NB_VGA_VDD — NB_VGA_VDD

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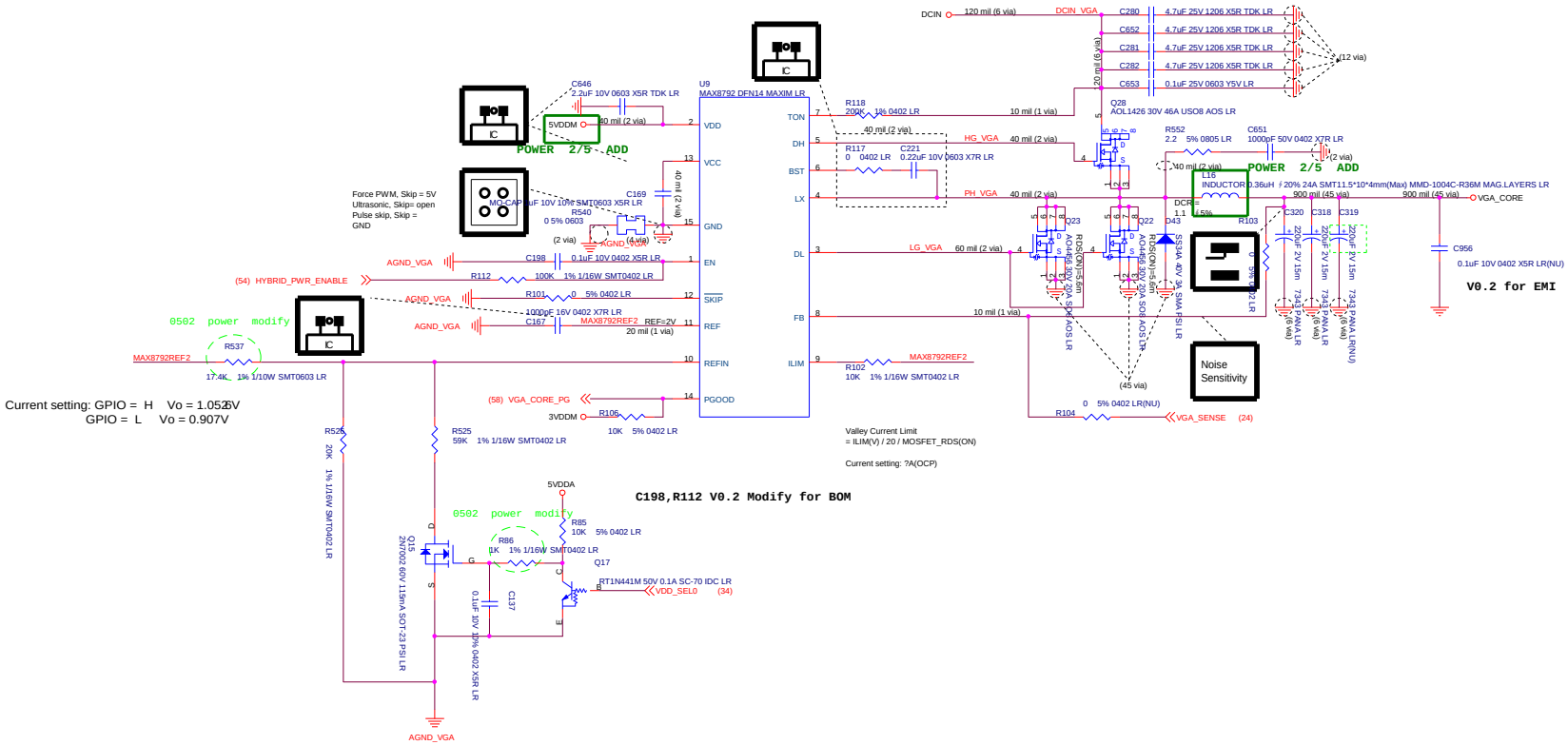
NB9P VGA Core



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Title	XY680>Penryn+Candiga GM45+ICH9M	
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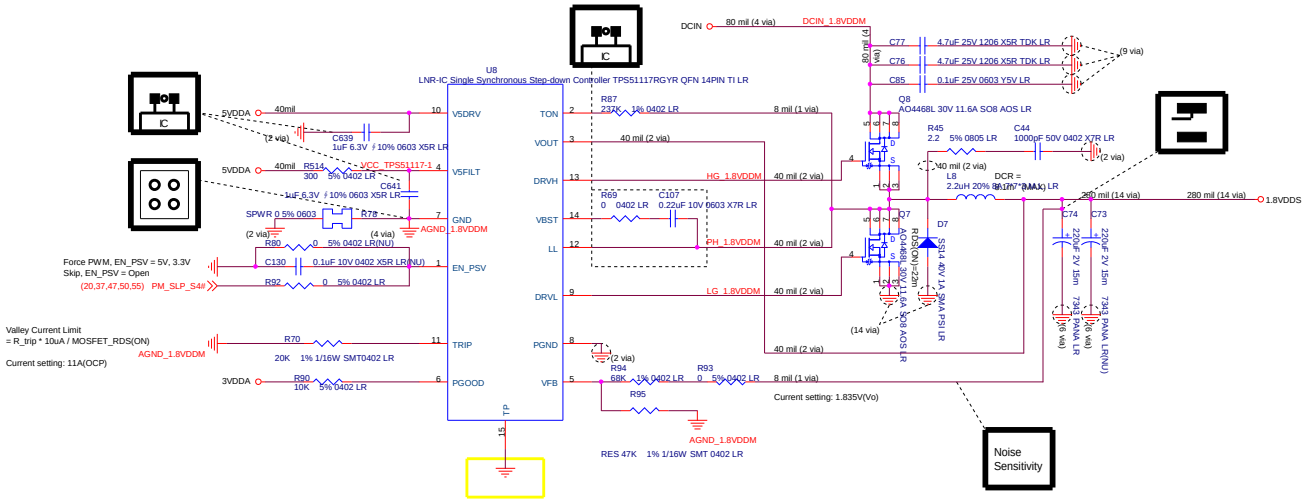
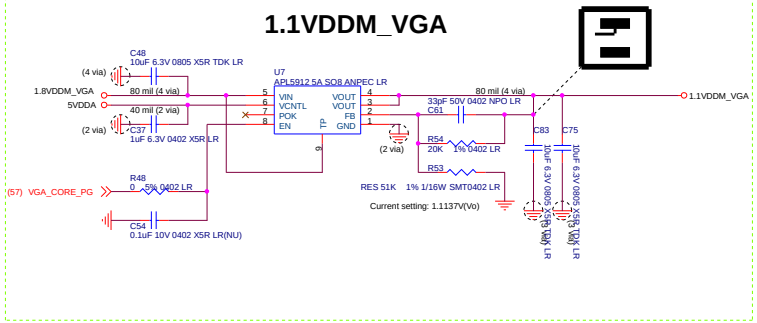
VDDR 1.8VDDS, 1.8VDDM_VGA, 1.1VDDM_VGA

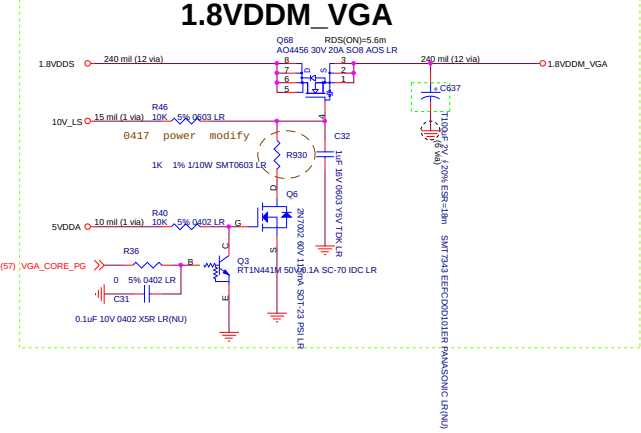
VDDR 1.8VDDS



1.1VDDM_VGA



1.8VDDM_VGA



(54,55,56) 10V_LS — 10V_LS

(32,52,54,55,56,57,59) DCIN — DCIN

(21,41,47,49,54,55,56,57) 5VDDA — 5VDDA

(8,18,20,21,22,24,32,37,38,39,41,45,47,48,49,50,52,54,55) 3VDDA — 3VDDA

(13) 1.8VDDS — 1.8VDDS

(24,25,29,33) 1.1VDDM_VGA — 1.1VDDM_VGA

(25,26,27,28,32,33) 1.8VDDM_VGA — 1.8VDDM_VGA

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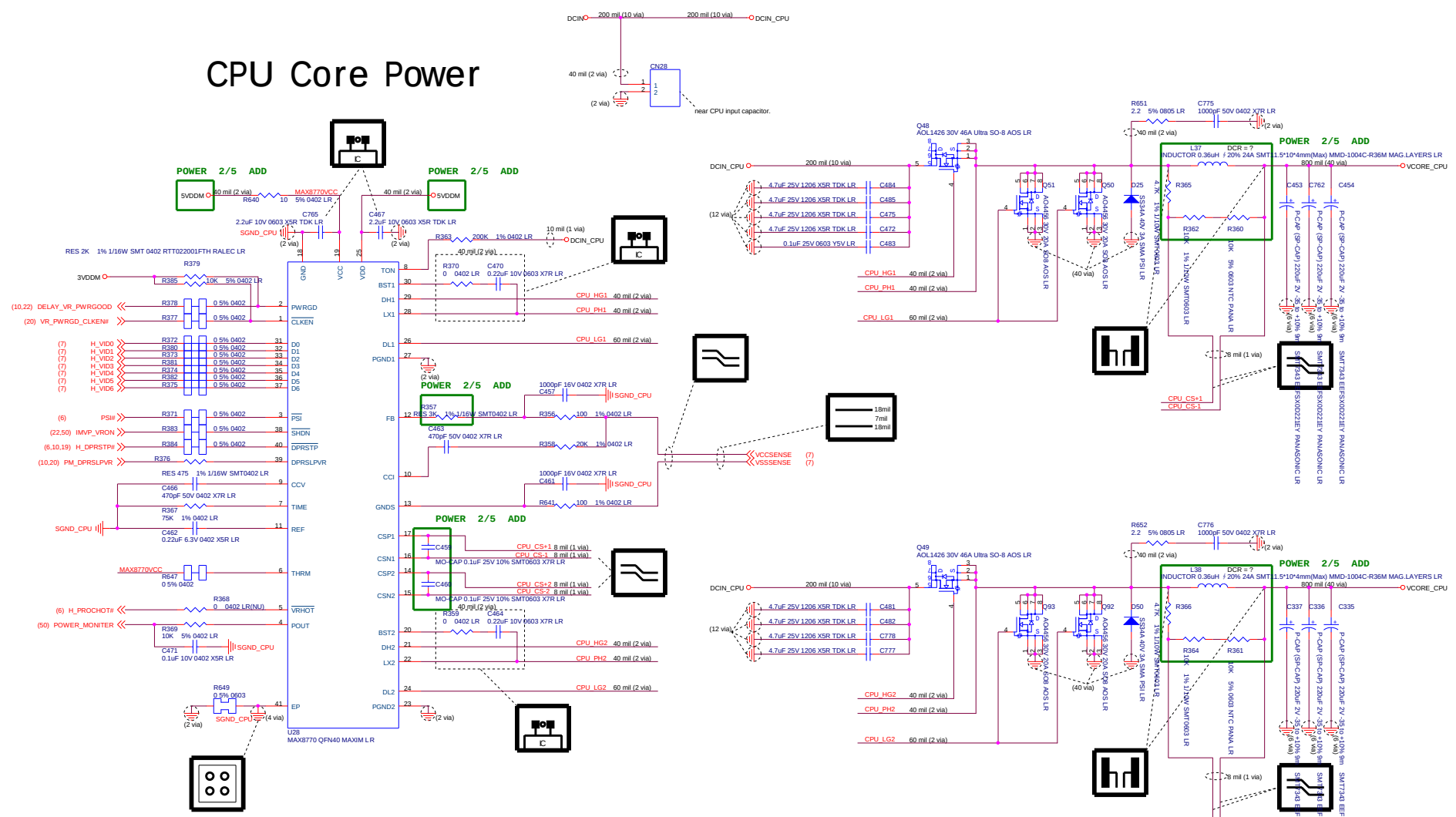
CPU Core Power



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Title		
Size: C	Document Number: CPU Core Power	Rev: 0.2
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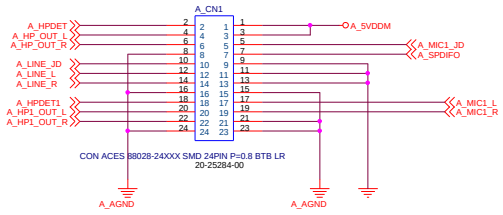
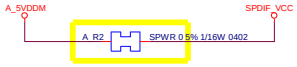
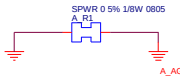
AUDIO CNN

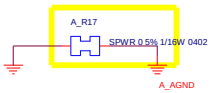




2008/05/13 Change to SPWR 0402



2008/05/13 Change to SPWR 0402
2008/04/23 Add for EMI



5/23 modified for Mic in Dynamic Range fail issue

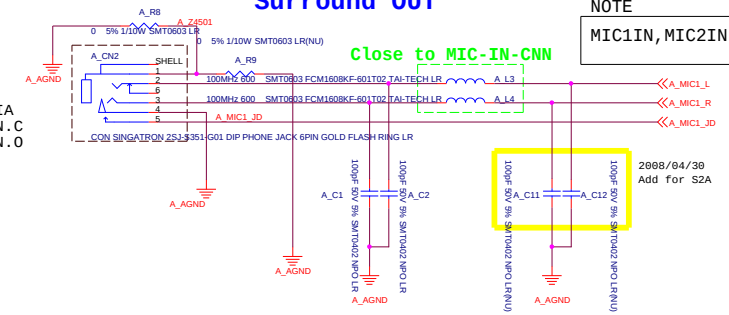
MIC IN
Surround OUT

Placement this Jack on middle

NOTE

MIC1IN,MIC2IN, MIC_JD,ﾏｲｸ AGROUND

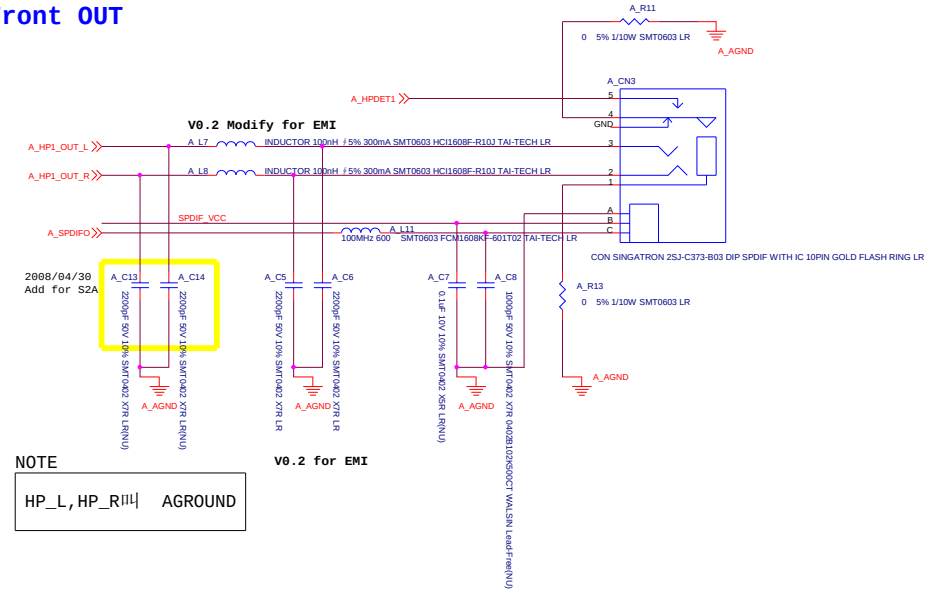
FOR AZALIA
2 AND 6 N.C
4 AND 5 N.O



2008/04/30
Add for S2A

HEADPHONE JACK/LINE OUT
Front OUT

Placement this Jack on notebook left side



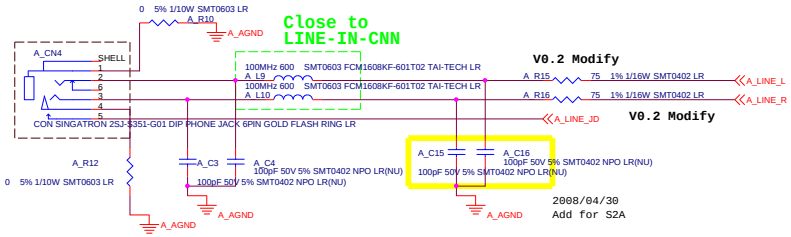
NOTE

HP_L,HP_Rﾏｲｸ AGROUND

V0.2 for EMI

LINE IN Center OUT

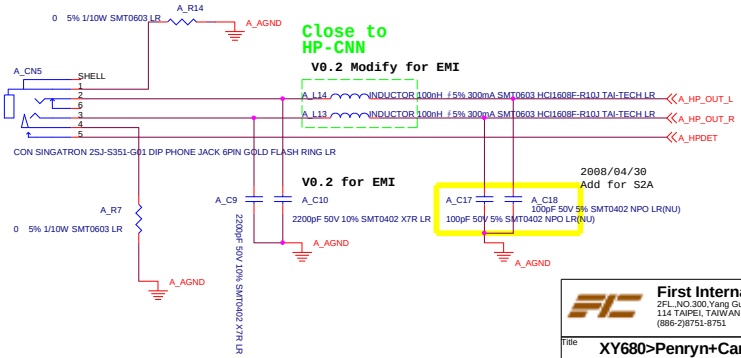
Placement this Jack on right side

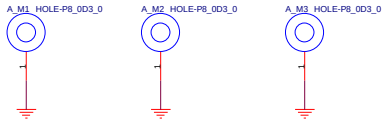


2008/04/30
Add for S2A

HEADPHONE JACK-2

Placement this Jack on left side





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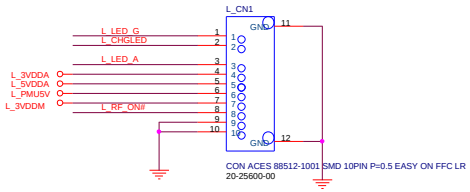
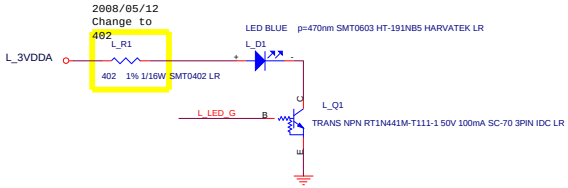
LED indicator control logic

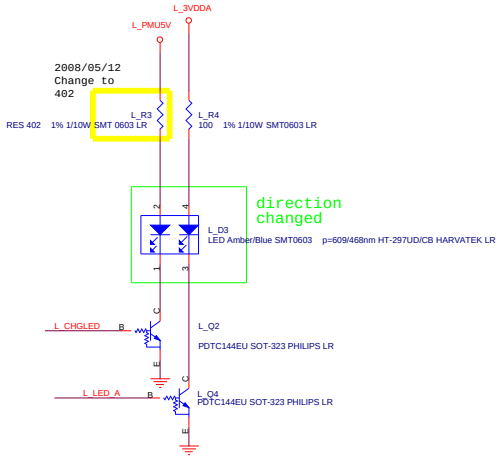
LED Board CON



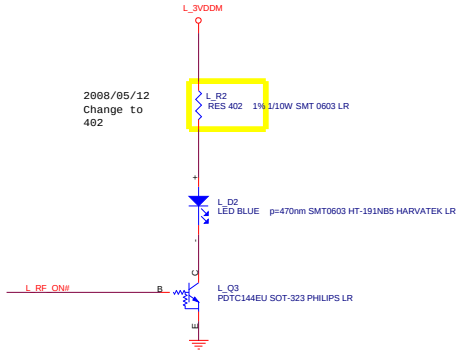
Power indicator

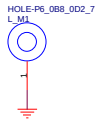


Charger indicator



Wireless indicator





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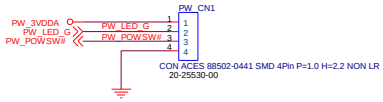

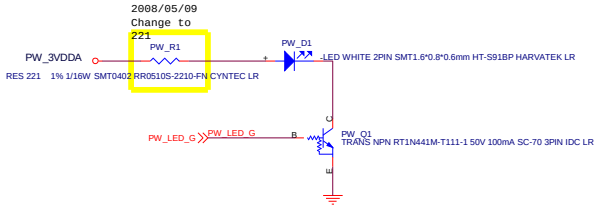

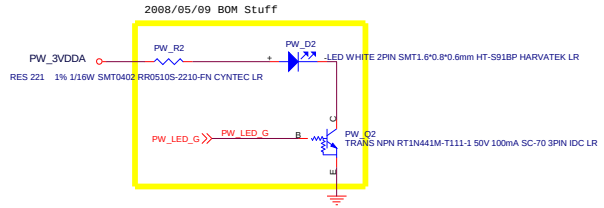

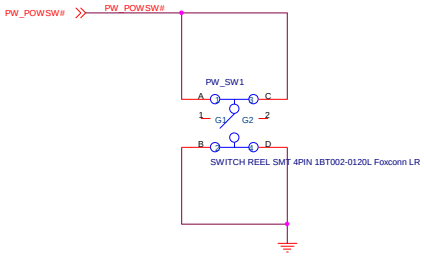

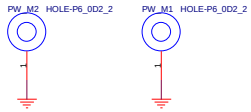

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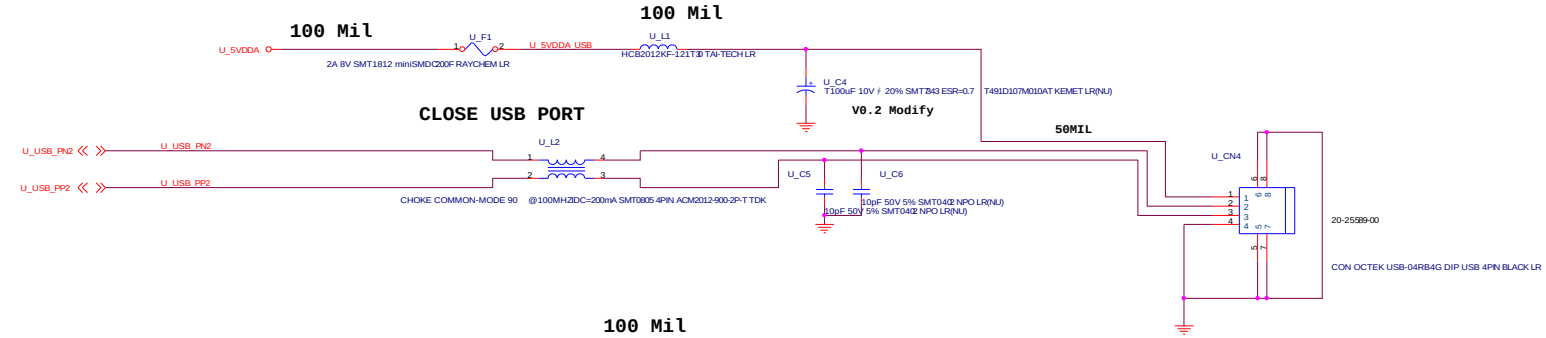
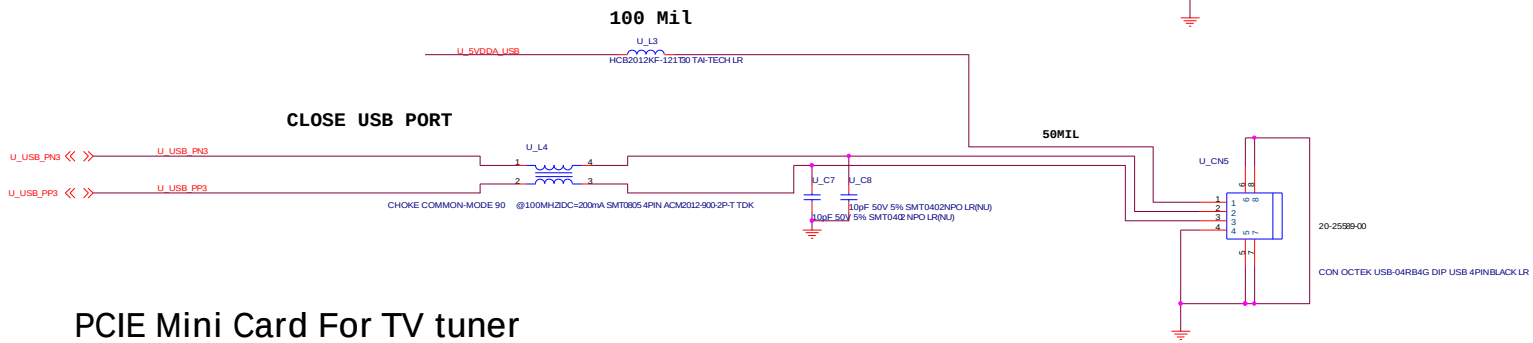
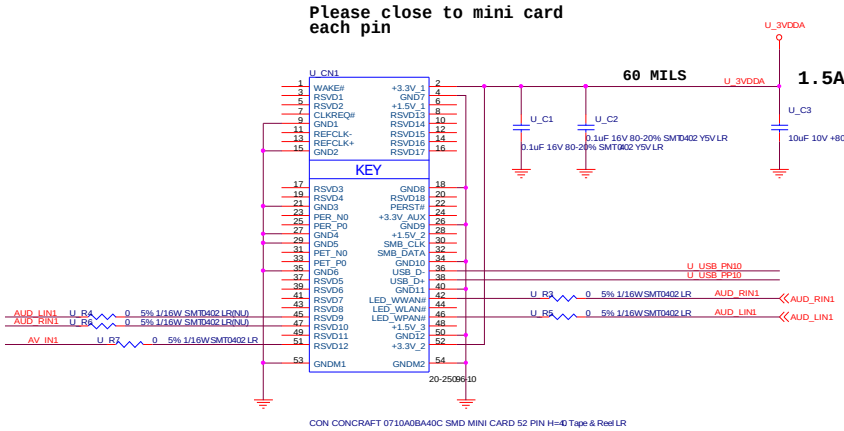
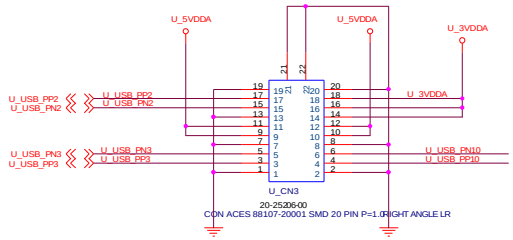
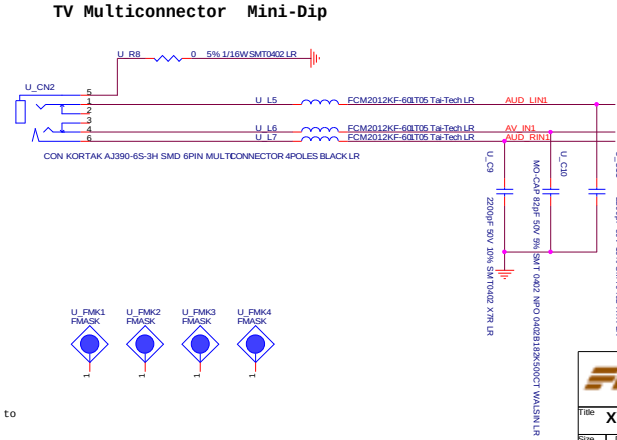


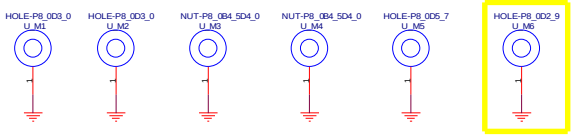


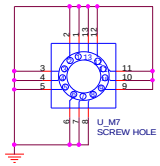
PCIE Mini Card For TV tuner

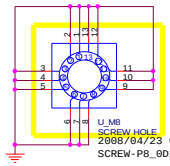












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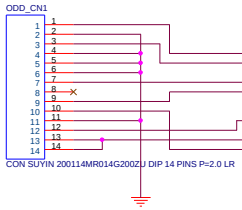
SATA ODD CN MALE



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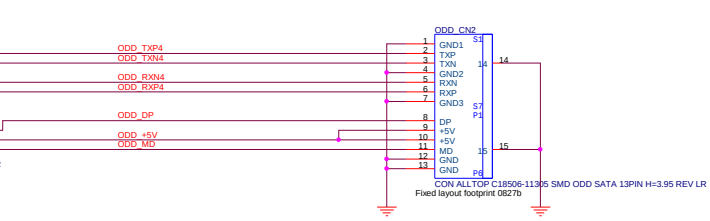

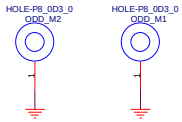

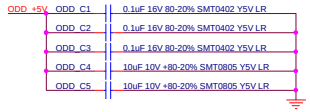

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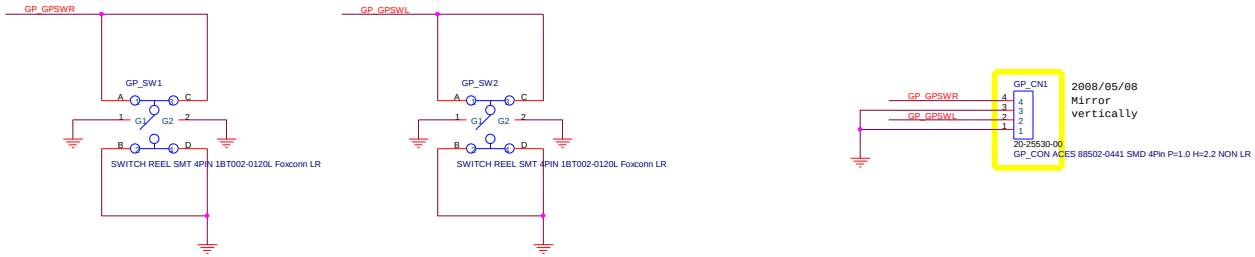

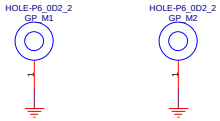

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